RE-ORDER NO. 65-335
APP. D

APPENDIX D

(LOCKED OSCILLATOR PHASE MODULATOR)

Submitted as part of the Final Report

for RF Test Console on CTL

Contract No. 950144

NAS 7-100

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PLC - PHASE MODULATOR ANALYSIS

This technical report is in response to the work description of Task 3910 for the RF Test Console (G.O. 36542). Design parameters which enable linear phase modulation of a locked oscillator by complex video signals are established by analysis. The driving signal is summed with the phase error to deviate the locked oscillator according to the basic block diagram of Figure 1.1, thereby producing a PM output at the carrier frequency.

As demonstrated in the analysis below, the system is feasible provided that (1) a phase detector having linear sawtooth characteristics is used, (2) the linearity and time constant of the deviable oscillator are adequate, and (3) a count-down frequency divider is used in the feedback channel to compress the wide phase deviation required within the linear range of the phase detector. (4) The linearity and frequency response of all loop components can be fabricated to the required accuracy. The latter requirement will have to be verified experimentally.

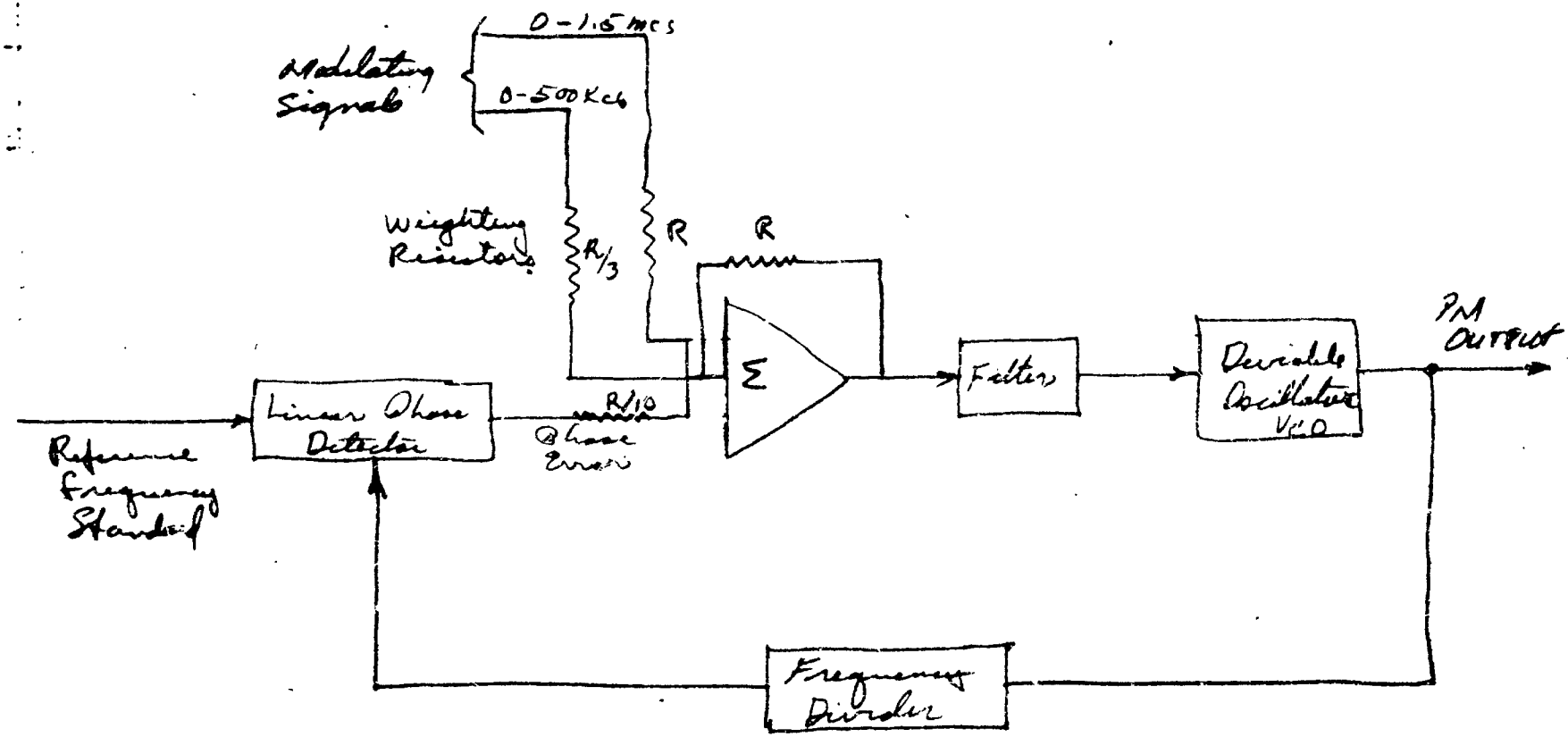


Fig 14 Basic Phase Locked FM Modulator

I PHASE MODULATOR REQUIREMENTS

A. Summary of Specifications (Reference JPL Spec No. GPG-15062-DSN)

The following pertinent specifications establish the basic requirements:

1. Transmitter center frequency - 50 mcs manually tunable ± 500 cps.

2. PM Operational Modes - Simultaneous narrow-band/large modulation index plus wide-band/small modulation index operation.

3. Reference Frequency Stability: Short Term: 1 part in 10^7 per minute.
   Long Term: 5 parts in 10^7 per 4 hour period.

4. Frequency Response - Narrow Band: ± 0.1 db from d-c to 500 kc
   Wideband: ± 0.5 db from 500 kc to 1.5 Mc

5. Phase Deviation at 50 mcs - Narrow band spectrum: ± 3 radians peak
   Wide band spectrum: ± 1 radian peak.

6. Phase Stability - 1 degree R.M.S. phase error in transmitter-receiver pair measured in a noise free phase-coherent receiver of $2B_L = .3$ cps bandwidth, as amended on 5 May 1964. 4

7. Fidelity - Two tone tests of transmitter-receiver pair: Spurious sidebands within the modulation bandwidth to be 40 db below the modulated carrier; or alternatively, 50 db below unmodulated carrier.

8. Deviation Linearity - Consistent with Fidelity requirement

9. Incidental AM - Consistant with Fidelity requirement

B. Analysis of Requirements

1. Peak Frequency Deviation: It is found that in order to comply with the phase deviation specified, peak frequency deviations of 1.5 and 2.0 mcs are required for the wideband and narrow band modulations respectively. Therefore, for the phase modulator of Figure 11, the VCO and its driving amplifier must have a dynamic range of at least ± 2.0 mcs at the 50 mcs output frequency.

2. Spectral Weighting of Modulating Signals : During simultaneous modulation the amplitude levels of the narrow band and wideband spectrums are weighted so that the deviation due to the

narrow band signal is 3 radians peak, while the deviation due to the wideband signal is 1 radian peak. Thus, the total composite peak phase deviation is 4 radians, Figure 1.2. The summing amplifi - in the forward circuit, Figure 1.1, must therefore accept two driving signals, one narrow band - one wideband, with three to one amplitude weighting of the respective signals. This is accomplished by adjustment of resistor values in the input and feedback networks of the operational summing amplifier.

3. Fidelity Allocations: The specification is given for a transmitter-receiver pair. For design purposes, the transmitter and receiver are treated separately, hence it is desirable to have separate objectives. Should the designer have complete freedom in the choice of subsystems, it is considered that slightly greater difficulty will be encountered in the transmitter than in the receiver. But the receiver system is specified in form and technique to be a simulation of the DSIF equipment. As will be shown below, the deviation and fidelity objectives require allowance for

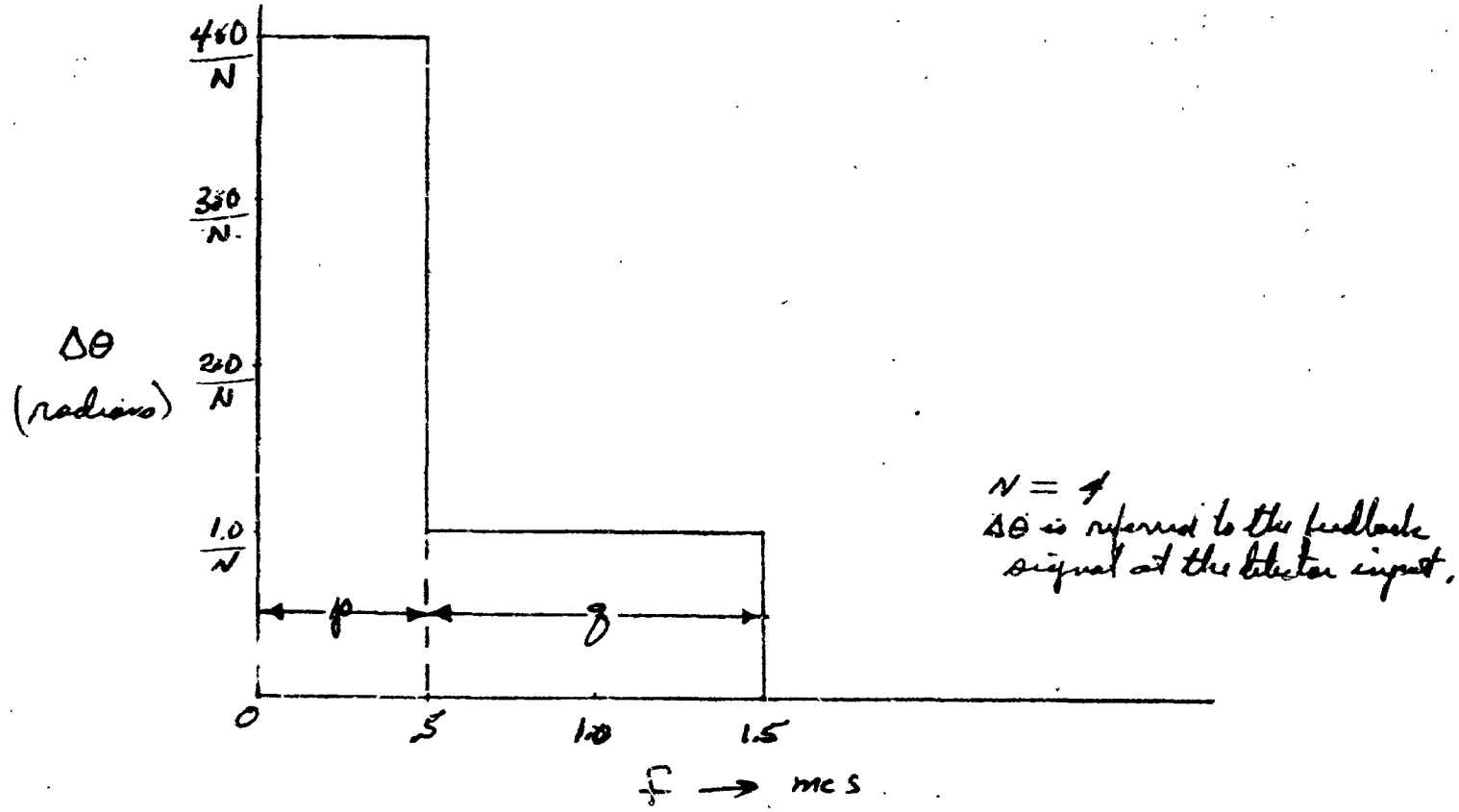


Fig. 2. Spectral Weighting, Two-Unequal-Tone Test

large intermodulation components at the output of the modulation detector. System performance need not be necessarily limited providing the tones of the modulating signal are carefully chosen to avoid frequency coincidence with intermodulation products.

With respect to the design of the phase modulator (transmitter), the intermodulation and in band spurious objectives will be taken at -46 and --56 db levels to admit equal degradation in the AM modulator, S/N summer and PM receiver.

C. Summary of Design Objectives

Objectives for a PLC phase modulator design are tabulated as follows:

1. Loop Characteristics:

Type I - 6 db per octave slope of open loop gain over the modulation band. Amplitude Frequency Response (closed loop) Flat 0.1 db to .05 mcs.

Delay vs. Frequency response (closed loop_ - less than 1 nanosec to 1.5 mcs (tentative)

Rejection at 25 mcs - 50 db

Spurious and inband intermodulation - 56 db below un-

Modulated carrier peak phase deviation - 4 radians

Velocity constant $K_V = 9.5 \times 10^6$

2. VCO:

Peak frequency deviation ± 2 mcs

Sensitivity >0.6 x 10^6 cycles per second - volt

Linearity - 2%

Q ≈ 12.5

Output Carrier Frequency - 50 mcs

3. Phase Detector

Linearized (Sawtooth) Characteristic

Phase Error Range - ± Pi radians

Linearity - 5%

Sensitivity - 1 volt per radian error

4. D-C Amplifier

Gain - 20 db

Linearity - 0.1%

Voltage Output Range - ± 10 v

Equivalent Corner Frequency - 15 mc

Drift 100 μv/wk

5. Loop Filter $F_1(s)$

(Lag) Quadratic

Resonant Frequency $W_{no} = 42 \times 10^6$ rps

Damping Coefficient, $\zeta_o = 0.53$

6. Feedback Frequency Divider Ratio, N = 4

7. Estimated transport lag around loop 20×10^{-9} seconds

8. Equalization Networks - To be specified.

II. LOOP DESIGN CONSIDERATIONS

In this section some fundamental relationships and basic concepts of phase-lock circuits, feedback control systems, and low pass filters are described in order to establish a logical design procedure and to support the mechanization proposed.

A. Optimization Criteria

The standards by which one measures the merit of a system must be selected with due consideration of the objectives of the system operating in its specific application. For the PLC - phase modulator the designer might consider several optimization criteria. For example, the designer might strive for minimal (a) modulation error, (b) intermodulation, or (c) noise bandwidth. The designer might also emphasize (1) optimum transient response, (2) maximally flat frequency response (with large out of band attenuation) or (3) optimally flat group delay (vs. frequency) response. It is certain that all of these desirable characteristics cannot be achieved in a single unique design.

Because the PLC - phase modulator operates in a "noise free" environment the minimization of noise bandwidth does not appear to have particular significance. Noise bandwidth should not therefore be given great emphasis in the modulator design. Efforts in this area should be limited to those necessary to assure the application of noise free modulating signals, pure reference signals and clean power supplies.

What is more important in this application is the minimization of both the modulation error and the intermodulation between tones of an ensemble of signals. These are both minimized by high open loop gain and wide loop bandwidths, however such a design must be tempered by the practical realization of the inherent limitations for stability considering the nonminimum-phase functions caused by system time delay plus the further requirement for attenuating harmonic products of detection within the loop.

While stability is not the principal objective it is nevertheless the limiting factor. Acceptable stability during transient forms of modulation would require a phase margin of about 60 degrees at the open

loop unity gain frequency.

Because the PLC - phase modulator is a feedback control circuit it possesses characteristics generally comparable to those of a low pass filter, having both an amplitude and phase versus frequency response. It is not sufficient to specify only that the device have a flat frequency response. Should the slope of the closed loop phase versus frequency response vary then delay distortion of the angular modulation occurs. To minimize modulation error and intermodulation a flat delay response is also required.

Should a compromise be required, it is our considered opinion that optimization of delay response should be emphasized to the detriment of frequency (amplitude) response, if necessary. This recommendation is based upon the fact that distortion caused by the inherent characteristic of the loop is most difficult to improve whereas compensation for variations of frequency (amplitude) response is possible by at least two methods, namely:

a) By weighting the spectrum of the modulating signal before its application to the phase modulator, and

b) By (amplitude equalization) after detection in the baseband circuits of the PM receiver, on a per channel or individual tone basis

The requirements of the overall system are nevertheless supreme. Should some unique characteristic of the applied signals (which have not been specified nor examined during the scope of this study) demand another result then the design possibilities are sufficiently flexible to accomodate an adjustment. Lacking specific signal definition, we select the criteria for a phase-locked phase modulator to be the minimization of modulation error and intermodulation by use of a "maximally" flat delay response, with loop gain and bandwidths consistent with the modulation spectrum and with adequate rejection of "spurious" harmonics of detection within the loop.

B. Fundamental Form - Type Filtering for Ideal PM:

In the circuit arrangement shown in Figure 1.1 the objective is to provide a high fidelity broad-band phase modulator capable of wide angular

deviation. In actuality the summing amplifier, filter, and VCO should be considered as a single physical subcircuit. An active filter is visualized. To achieve broadband modulation a low-Q VCO might be specified, however extremes should be avoided. In the practical design the VCO should be assumed to have finite bandwidth, hence its control time constant should be a factor in the loop frequency response.

A simplified mathematical model of the PLC - Phase modulator is given in Figure 2.1, wherein the phase detector is assumed to possess linearity over the range of maximum error signals and that distributed time delays are negligible. The corner frequency, W_1, is due to the limited response of the driving amplifier and VCO control circuit. Under these conditions the PM output, $\Delta\theta_o$, as a function only of the modulation may be written as:

$$\Delta\theta_o(s)\Big|_{V_M(s)=0} = \frac{K_A K_{VCO}\ F_1(s)\ \ V_M(s)}{S\left(\frac{S}{\omega_1}+1\right)\left[1 + \frac{K_A K_d K_{VCO}\ F_1(s)}{N\ S\left(\frac{S}{\omega_1}+1\right)}\right]} \qquad \text{Eq (2.1)}$$

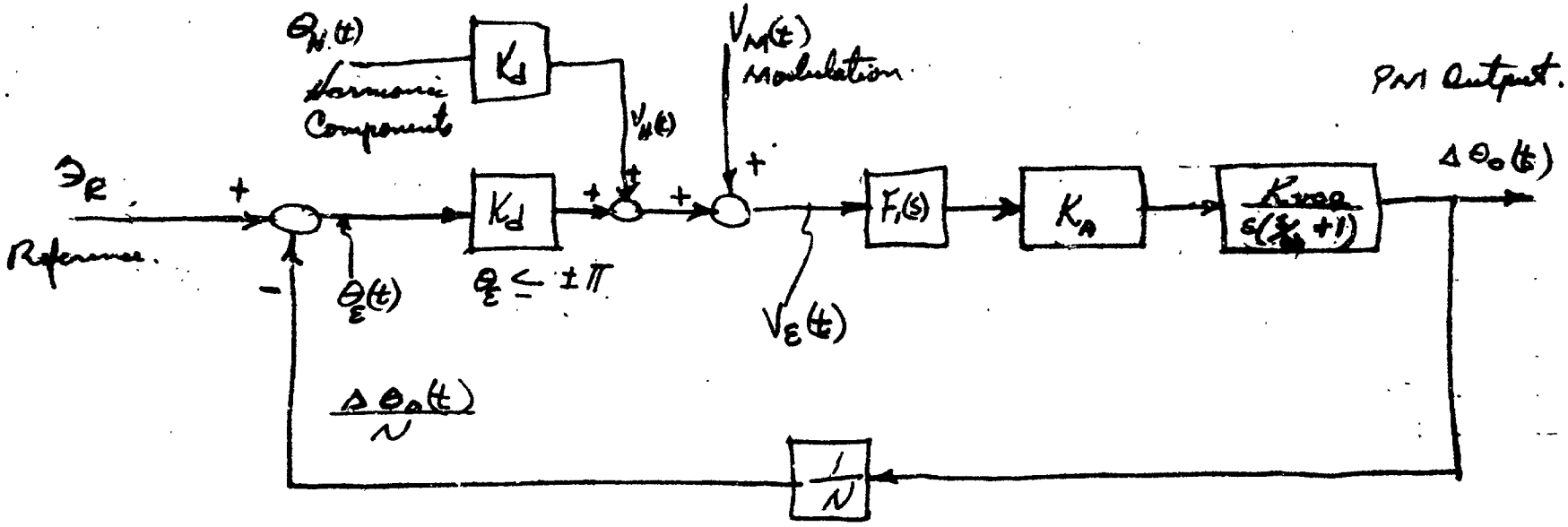


Fig 2. Elementary PLC - Phase Modulator Equivalent Diagram.

or,

$$\left.\Delta\theta_o(s)\right|_{V_H(s)=0} = \frac{N}{K_d}\,\frac{V_M(s)}{\frac{s}{K_v}\,\frac{\left(\frac{s}{\omega_1}+1\right)}{F_1(s)}+1}, \qquad (2.2)$$

where

$$K_v = \frac{K_A\,K_d\,K_{VCO}}{N}. \qquad (2.3)$$

But before conclusions are drawn as to the character of the filter, $F_1(S)$, we must consider its secondary function, namely that of suppressing harmonics generated by the mixing process within the phase detector. As a function only of these harmonics, we have also

$$\left.\Delta\theta_o(s)\right|_{V_M(s)=0} = \frac{N}{K_d}\,\frac{V_H(s)}{\frac{s}{K_v}\,\frac{\left(\frac{s}{\omega_1}+1\right)}{F_1(s)}+1} \qquad (2.4)$$

Thus from Equations (2.2) and (2.4) the designer would appear to be faced with a dilemma in the choice of $F_1(S)$ for in Equation (2.2) it is desired that the PM output be directly proportional to, and a linear function of the modulating signal, V_M, at all frequencies

within its band. This would be assured if the gain constant K_v were large compared to the maximum modulating frequency ($S = jW_{max}$) and if $F_1(S)$ provided lead compensation to counteract the lag corner (W_1) introduced by the VCO control. From a modulation point of view equation (12) would be reduced to:

$$\Delta\theta_o(s) = \frac{N}{K_d} \frac{V_M(s)}{\left[\frac{S}{K_v} + 1\right]} \quad \ldots \quad (2.5)$$

However for broadband modulation a conflicting requirement arises in Equation (2.4). The output signals, $V_H(s)$, of the phase detector occurring at the fundamental reference frequency and its harmonics should be suppressed in level prior to modulation upon the PM (VCO) output. Because of the wide peak phase deviation specified (4 radians) a feedback divider (of ratio $\frac{1}{N}$) sets the operating frequency of the phase detector only a few octaves above the modulation spectrum. The following alternatives are available to the designer.

First, lead compensation $F_1(s) = \left(\frac{S}{w_1} + 1\right)$ could be selected for optimum response to the modulation input in which case

the FM output would have the full amplitude of harmonic distortion. Secondly, no filtering whatsoever $F_1(S) = 1$ could be selected in which case the harmonic distortion would be attenuated only by the response of the VCO control circuit. Thirdly by limiting the frequency response to a minimum bandwidth approximately equal to the modulation spectrum of V_M, further filtering of the harmonic signal, $V_H(s)$, may be provided by choosing a lag filter, where the parameters are appropriately chosen so as to ensure loop stability, yet with desirable loop delay characteristics.

In the first and second alternatives, bandpass filters would be required to remove the spurious modulation due to the harmonic signal, V_H. These filters would require a linear phase vs frequency characteristic to avoid delay distortion of the modulated signal.

On the other hand, the third alternative, if careful design procedures are employed, can provide the desired result. The lag concept

is preferred because: (a) its cost is small compared to that of post-modulation bandpass filtering, (b) it maximizes the energy within the desired PM output spectrum by pre-modulation filtering, and (c) it avoids saturation of the amplifiers required in the forward channel of the loop.

C. Loop Design in the Complex Frequency Plane:

In this section three possible design procedures are presented. These include feedback control design concepts based upon (a) the use of Bode and Nichols charts as typically used in servo design, (b) the use of Butterworth filter synthesis to produce a maximally flat amplitude vs. frequency response, and (c) the use of constant delay approximations. A comparative analysis of the characteristics and performance of the resulting designs suggests a need for careful and detailed specification of phase modulator requirements.

1. Use of Bode and Nichols charts-Asymptotic Design: A conventional feedback design procedure has been used in pre-

paration of a preliminary design for basic analysis of the loop feasibility. . The use of graphical techniques based upon the logarithmic (numerical) gain vs frequency (or Bode) diagram and the logarithmic gain vs linear phase angle (Nichols') chart are simple in application and effective in rapid synthesis of desired characteristics based upon a chosen form of open loop transfer function. The accuracies obtained with the procedure are sufficient for the majority of servo-design problems. In the paragraphs to follow the design is based upon the frequency response, signal bandwidth, and spurious attenuation requirements specified for the modulator.

In applying the Nichols chart (see for example any standard textbook on linear feedback theory) it is well known that peaking in the steady state frequency response of the closed loop is indicated by tangency of the locus of the open loop transfer function to an M_p contour of constant magnitude. Thus for a specified flatness of frequency response of $\pm$ .5 DB the open loop locus must reach unity gain in the manner illustrated in Figure 2.2 with a phase margin of approximately

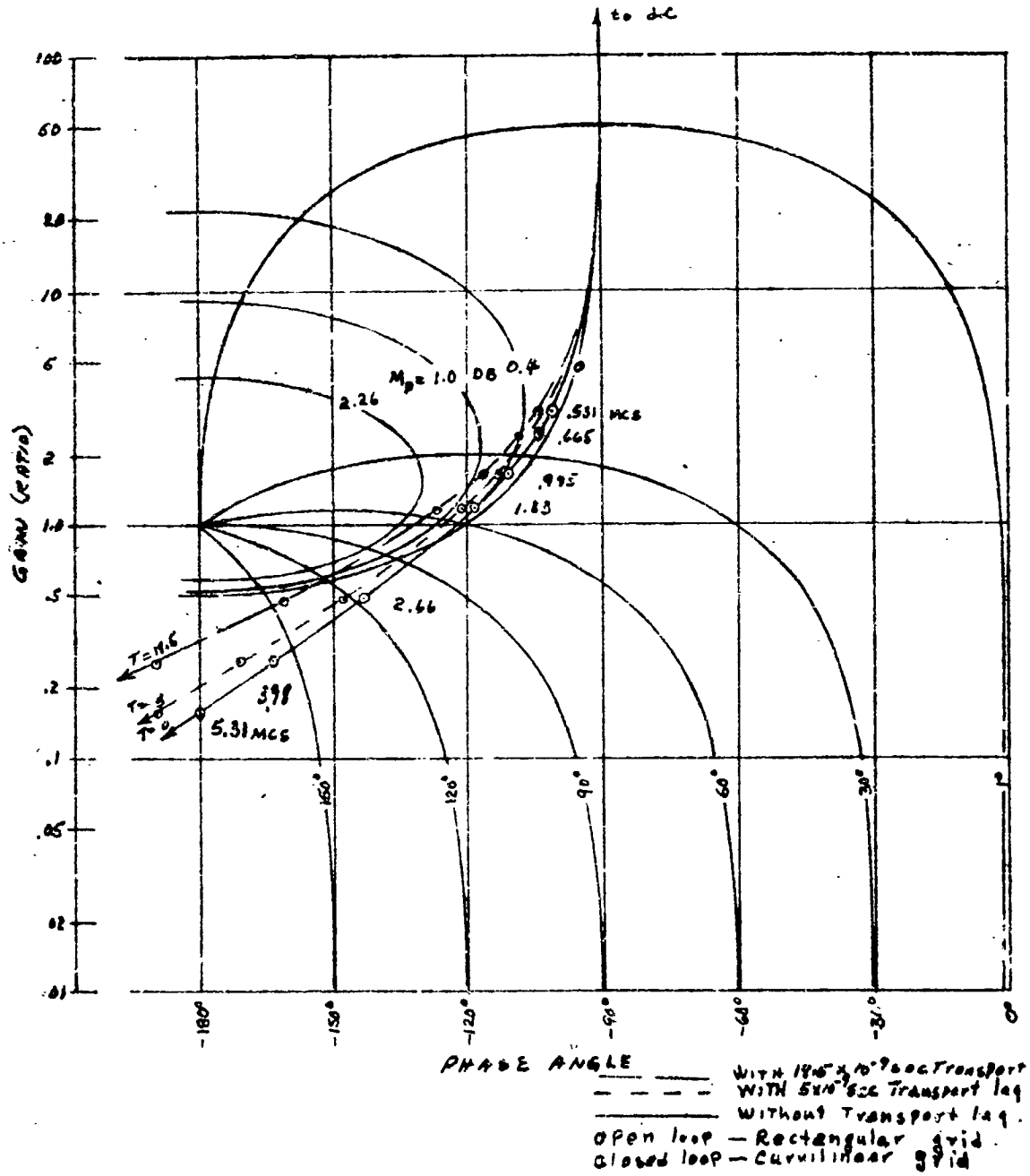


Fig. 2.2 GAIN-PHASE PLOT OF PLC-PHASE MODULATOR FREQUENCY RESPONSE

55-60 degrees. In order to illustrate the method, we select for the quasi-linear model of Figure 2.1 a lag filter comprising a single time constant also at a corner frequency, W_1. We may write the open loop transfer function as:

$$G(s) = \frac{K_v}{s\left(\frac{s}{\omega_1}+1\right)^2} \qquad (2.6)$$

where $$K_v = \frac{K_A K_d K_{VCO}}{N} \qquad (2.7)$$

The gain vs frequency response can be determined from

$$|G(s)| = \left[G(s) \cdot G(-s)\right]^{\frac{1}{2}} \qquad (2.8)$$

which upon substitution of Equation (2.6) becomes.

$$|G(j\omega)| = K_v \left\{ \frac{1}{\omega^2\left[\left(\frac{\omega}{\omega_1}\right)^4 + 2\left(\frac{\omega}{\omega_1}\right)^2 + 1\right]} \right\}^{\frac{1}{2}} \qquad (2.9)$$

or alternatively,

$$|G(j\omega)|_{db} = +20\log_{10} K_v - 20\log_{10}\omega - 10\log_{10}\left[\left(\frac{\omega}{\omega_1}\right)^4 + 2\left(\frac{\omega}{\omega_1}\right)^2 + 1\right] \qquad (2.10)$$

The phase angle vs frequency (ignoring transport lag at this time) is simply:

$$\beta = -\frac{\pi}{2} - 2\arctan\frac{\omega}{\omega_1}, \text{ radians.} \qquad (2.11)$$

The phase margin ϕ_m is equal to π radians minus the phase angle, B_c, accumulated at the unity gain frequency for the open loop, thus

$$\phi_m = +\frac{\pi}{2} - 2\arctan\frac{\omega_c}{\omega_1}, \text{ radians} \qquad (2.12)$$

The recommended phase margin of 60 degrees is selected for acceptable stability in presence of binary or transient modulation signals and for peaking in the frequency response of about $\pm$ .5db maximum. We can solve for the corner frequency, W_1 :

$$90^\circ - 60^\circ = 2\arctan\frac{\omega_c}{\omega_1}$$

$$\frac{\omega_c}{\omega_1} = \tan 15^\circ$$

$$\omega_1 = 3.73\,\omega_c \quad , \text{ or } \omega_1 = 3.73\,K_v \qquad (2.13)$$

The next step is to determine the open loop bandwidth, W_c. The required value for W_c is determined by, (a) the gain required at the top of the modulation band (near $\omega = 2\pi \times 1.5 \times 10^6$ cps) for the suppression of intermodulation components (see Table 4 and the discussion under SeeIII B2 below), and (b) the attenuation required

to reduce the spurious levels, caused by phase detector carrier feed-through and harmonics, to a level 50db below the unmodulated carrier.

According to the two-tone analysis of a 5% linear phase detector of range $\pm\pi$ radians the intermodulation due to the detector nonlinearity requires negligible gain to meet the fidelity specification. If this detector is achieved then the open loop bandwidth, W_c, can be calculated on the basis of (b), the attenuation at 25 mcs. From the geometry of Figure 2.3 it is obvious that

$$\left(\frac{f_1}{25}\right)^3 = \frac{0.003}{0.31} \qquad (2.14)$$

$$f_1 = 5.31 \text{ mcs}$$

$$\omega_1 = 2\pi f_1 = 33.4 \times 10^6 \text{ rps}$$

$$f_c = \frac{5.31}{3.73} = 1.43 \text{ mcs}$$

$$\omega_a = 2\pi f_c = 8.98 \times 10^6 \text{ rps}$$

$$K_v = 8.98 \times 10^6 \text{ sec}^{-1}$$

From Equations (2.3) and (2.7)

$$K_v = \frac{K_A K_s K_{VCO}}{N}$$

We have previously recommended:

$N = 4$ (See III A below)

$K_A = 10$ (See III B1 below)

Therefore $K_d K_{VCO} = \frac{8.98 \times 10^6 \times 4}{10}$

$K_d K_{VCO} = 3.59 \times 10^6$

If the detector sensitivity $K_d = 1$ volt per radian phase error

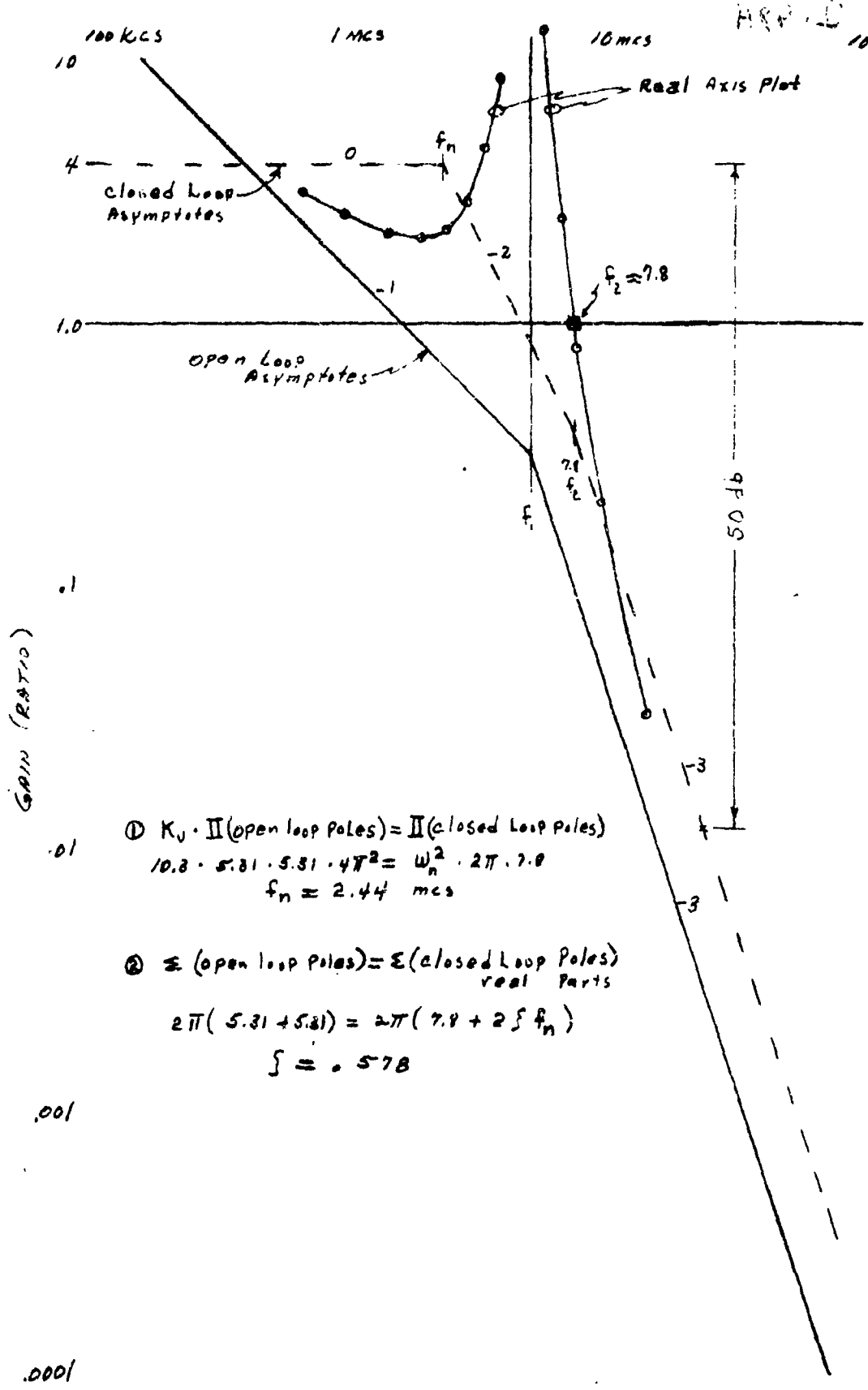
and $K_{VCO} = 3.59 \times 10^6$ radians per second-volt,

then in closed loop operation the PM output

$\frac{\Delta\theta_o}{V_M}(s) = 4.0$ radians peak within the

modulating band.

Further computations show that the selected parameters for the basic loop provide a desirable frequency response without the assistance of suggested pre-emphasis. A graphical solution was performed first to determine the roots of the closed loop equation and the peaking of its frequency response. The graphical solutions are given in Figures 2.2 and 2.4. These approximate solutions were confirmed by a more rigorous



① $K_v \cdot \Pi(\text{open loop poles}) = \Pi(\text{closed Loop poles})$

$10.8 \cdot 5.81 \cdot 5.31 \cdot 4\pi^2 = \omega_n^2 \cdot 2\pi \cdot 7.8$

$f_n = 2.44$ mcs

② Σ (open loop poles) $= \Sigma$ (closed Loop Poles) real Parts

$2\pi(5.31 + 5.81) = 2\pi(7.8 + 2\zeta f_n)$

$\zeta = .578$

Fig. 3.4 Graphical Analysis of PLL- Phase Modulator.

analytical computation of the closed loop frequency response which is shown in Figure 2.5.

The closed loop transfer function given above can be expressed in more general form as:

$$\frac{\Delta\Phi_o}{V}(s) = \frac{N}{\left(\frac{s^2}{\omega_n^2} + \frac{2\zeta}{\omega_n} s + 1\right)\left(\frac{s}{\omega_2} + 1\right)} \qquad (2.15$$

In Figure 2.4 values for the parameters ζ, W_n, and W_2 are determined from the open loop asymptotes and the real axis plot. The complex roots were found at a resonant frequency of 2.44 mcs with a damping coefficient of 0.578 . The upper lag corner f_2 in the closed loop is at approximately 7.8 mcs.

Having determined f_2, f_n, and ζ the closed loop asymptotic plot may be drawn which clearly shows a -50 DB attenuation at 25 mcs relative to the low pass signal spectrum.

The frequency response of the closed loop might be estimated by reference to any standard text on control theory, which have graphical

frequency responses for quadratic or complex roots. Estimates may also be made using the gain-phase plot of Figure 4, where the curvilinear grid represents the closed loop performance. From this plot maximum peaking of the order of 0.4 DB or less will occur at about 1.3 mcs as shown by the tangency of the focus to the M_p contour.

In view of the very tight specification on frequency response, i.e., less than $\pm$ .1 DB at 500 K_{cs} and $\pm$ .5 DB at 1.5 mcs, it was deemed advisable to compute the frequency response analytically, from

$$\left|\frac{\Delta\theta}{V_m}(j\omega)\right| = \left[\frac{\Delta\theta}{V}(s)\ \ \frac{\Delta\theta}{V}(-s)\right]^{\frac{1}{2}}$$

$$\left|\frac{\Delta\theta}{V_m}(j\omega)\right| = \frac{N}{K_d}\left[\frac{1}{\frac{\omega^6}{K_v^2\omega_1^4} + \frac{2\omega^4}{K_v^2\omega_1^2} + \frac{1}{K_v}\left[\frac{1}{K_v} - \frac{4}{\omega_1}\right]\omega^2 + 1}\right]$$

or alternatively,

$$\left|\frac{\Delta\theta}{V_m}(j\omega)\right|_{db} = 20\log_{10} N - 10\log_{10}\left\{\left(1 - \frac{2\omega^2}{K_v\omega_1}\right)^2 + \frac{\omega^2}{K_v^2}\left[1 - \left(\frac{K\omega}{\omega_1}\right)^2\right]^2\right\} \quad \text{Eq (2.16)}$$

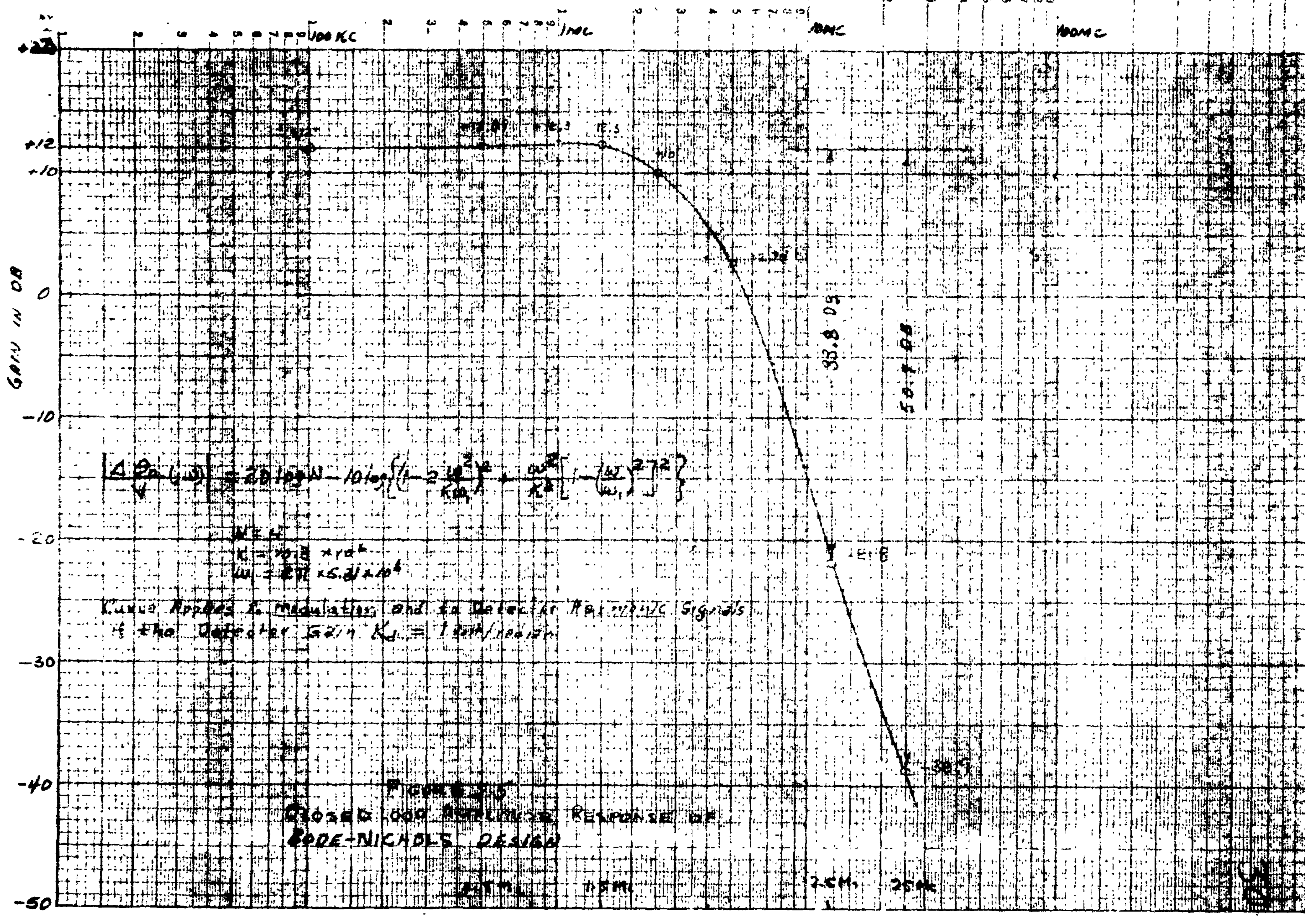


FIGURE [illegible]
CLOSED LOOP AMPLITUDE RESPONSE OF
BODE-NICHOLS DESIGN

where K_d = 1 volt per radian. This equation is written in terms of the open loop design parameters N, K_v, and W_1. It does not involve the inaccuracies of the graphical method. From the curve of Figure 2.5 it is seen that excellent correspondence with graphical estimates resulted. The relative attenuation at 12.5 and 25 mcs was calculated to be -33.8 and -50.9 DB respectively.

Study of Figure 2.5 reveals that a satisfactory amplitude vs frequency response may be obtained by simple synthesis procedures, using Bode and Nichol's diagrams, especially where the open loop transfer function consists of simple polynomials.

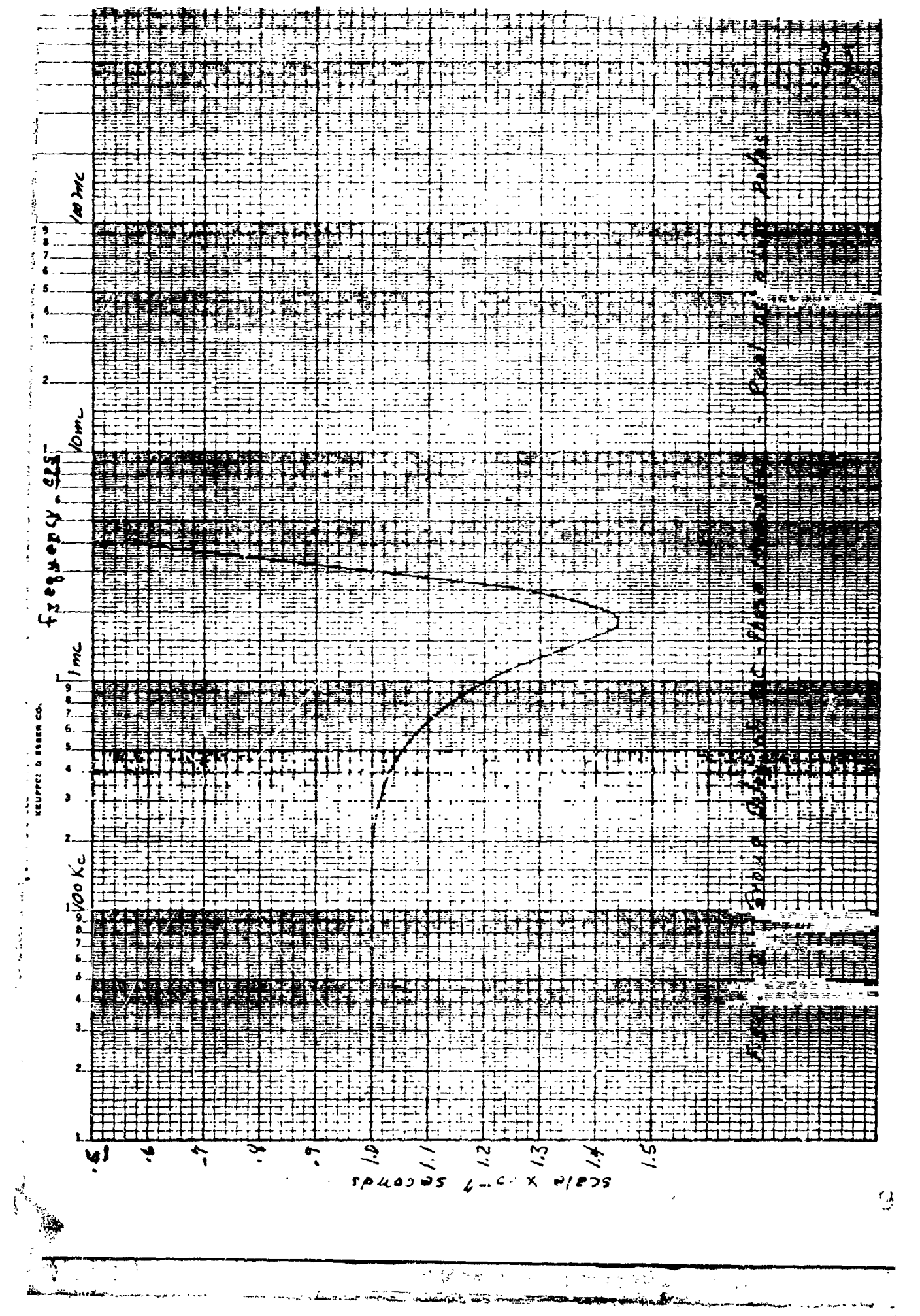
The phase response of the modulator may be calculated by use of the arctangent of the ratios of imaginary to real parts of the closed loop transfer function, as evaluated at frequencies of interest. The phase response is shown graphically in Figure 2.2 from the open loop data. Using the curvilinear grid of Figure 2.2, the closed loop phase response varies from zero to about -60 degrees over the 1.5 mcs bandwidth of the modulating signal.

The group (time) delay caused by the low pass characteristic of the phase modulator loop, having the suggested parameters, was calculated accurately and is plotted in Figure 2.6. The variation in group delay over the frequency range up to 1.5 mcs is seen to be less than 40 nanoseconds. Over the narrow band channel 0-500 Kcs, the variation of group delay is about 5 nanoseconds.

2. Design for maximally flat frequency response:

It has been suggested that loop synthesis using the Bode and Nichol's diagrams as illustrated in (1) immediately above is overly conservative in that improvements in flatness of amplitude response over the desired band and greater attenuation to out-of-band harmonics and spurious signals should be possible. Butterworth filter synthesis procedures are suggested as a possible phase-locked phase modulator design technique.

To obtain a Butterworth characteristic the procedure requires the synthesis of closed loop poles, complex and real, lying on a semicircle in the left half of the complex frequency plane. A fundamental constraint

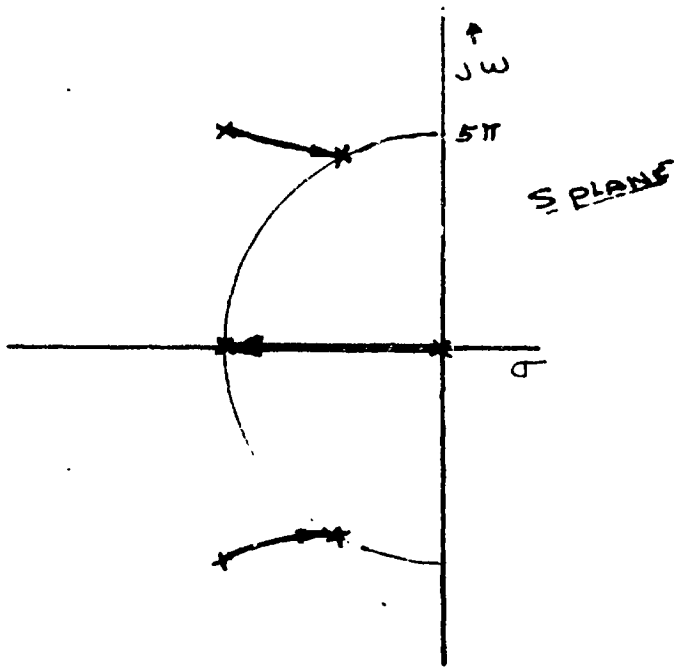

Frequency - cps
100 mc
10 mc
1 mc
100 Kc
Scale x 10^-7 seconds
0.5
0.6
0.7
0.8
0.9
1.0
1.1
1.2
1.3
1.4
1.5
KEUFFEL & ESSER CO.

upon the design exists because of the inherent pole at zero frequency which is a necessary requirement for the open loop transfer function of all phase-locked circuits.

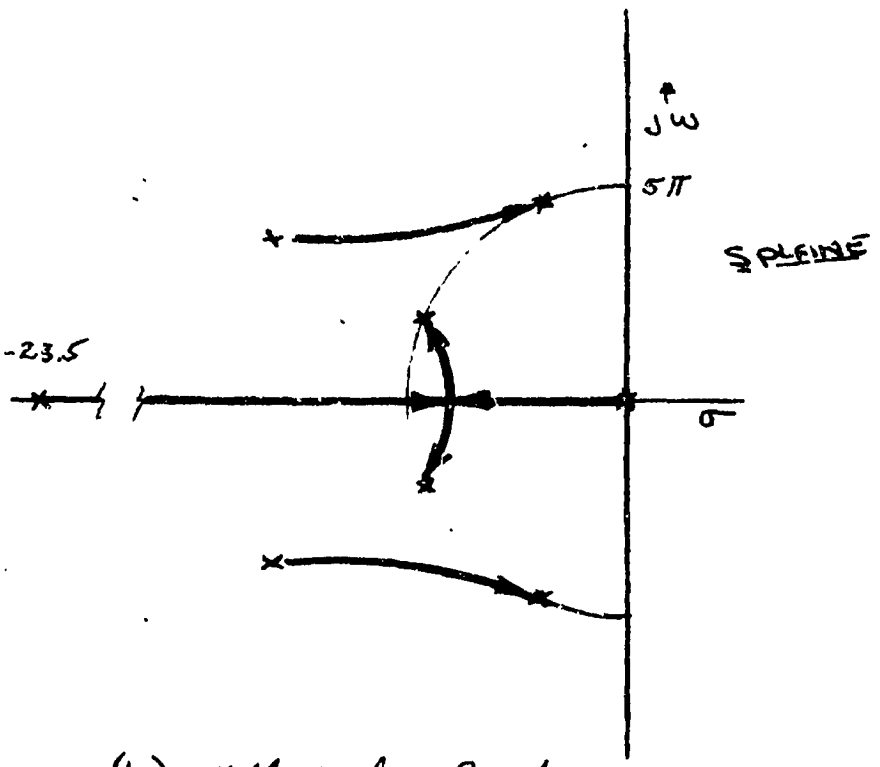
By judicious choice of loop gain and loop filter ($F_1(s)$) characteristics, it is hypothesized that open loop poles may be forced to assume a Butterworth distributions as illustrated in Figure 2.7.

From the root locus diagrams one may surmise that odd order Butterworths may be readily synthesized with phase lock systems having the inherent pole at zero plus loop filtering by complex pole networks. On the other hand even order Butterworth phase-locked circuit designs require an additional pole on the real axis which, with proper gain determination, combines with the inherent pole at zero to form a complex pair on the Butterworth semicircle.

For example, the transfer function for a <u>three pole Butterworth</u> response of the phase modulator output as a function of the input modulating signal is by definition:



(a) 3rd order System



(b) 4th order System

Fig 2.7 Butterworth Phase-Locked Phase Modulator – Root Locus.

$$F_3(s) = \frac{\Delta\theta_o}{N V_M}(s) = \frac{1}{\left(\frac{s}{\omega_n}+1\right)\left(\frac{s^2}{\omega_n^2}+\frac{2\zeta}{\omega_n}s+1\right)} \qquad (2.17)$$

The phase-locked circuit requires a pole at zero in its open loop transfer function. Since the total number of poles must be equal in the open and closed loop functions, we select the open loop transfer function as:

$$G_3(s) = \frac{K_v}{s\left(\frac{s^2}{\omega_{no}^2}+\frac{2\zeta_o}{\omega_{no}}s+1\right)} \qquad (2.18)$$

A closed loop transfer function may now be written in terms of open loop parameters by substitution in the familiar relation $F(s) = \frac{G(s)}{1+G(s)}$ so that:

$$F_3(s) = \frac{1}{\frac{s}{K_v}\left(\frac{s^2}{\omega_{no}^2}+\frac{2\zeta_o}{\omega_{no}}s+1\right)+1} \qquad (2.19)$$

By equating the closed loop relationships described by Equations (2.17) and (2.19) and solving for open loop parameters, we may synthesize a phase-locked modulator having the Butterworth characteristic. The equality is:

$$\frac{s^3}{K_v\omega_{no}^2}+\frac{2\zeta_o}{K_v\omega_{no}}s^2+\frac{s}{K_v}+1 = \frac{s^3}{\omega_n^3}+\frac{2\zeta+1}{\omega_n^2}s^2+\frac{2\zeta+1}{\omega_n}s+1 \qquad (2.20)$$

The conditions for equality requires that the coefficients of like power must be equal, therefore

For a 3rd order Butterworth design:

$$K_v = \frac{\omega_n}{2\zeta + 1} \qquad (2.21)$$

$$\omega_{no} = \omega_n \sqrt{2\zeta + 1} \quad , \text{ and} \qquad (2.22)$$

$$\zeta_o = \frac{\omega_{no}}{2\omega_n} \qquad (2.23)$$

In order to completely design the 3rd order Butterworth response the only determination necessary is to select a value of ω_n for the desired flatness over a given bandwidth. The coefficient of damping is uniquely determined for any design because of the uniform and symmetrical distribution of poles on the unit Butterworth circle. For the 3rd order Butterworth the coefficient is

$$\zeta = 0.5.$$

The value for the resonant frequency , ω_n , of the Butterworth may be selected from the published normalized curves. (See for example

"Reference Data for Radio Engineers", 4th Edition, chap. 7, page 194, (a book published by ITT Corp.). For a droop in the amplitude frequency response of 0.2DB at 1.5 mcs the standard normalized curve for the 3rd order Butterworth indicates a required value of

$$\omega_n = 5\pi \times 10^6 \text{ rps}, \text{ consequently}$$
$$K_v = 2.5\pi \times 10^6 \text{ sec}^{-1}$$
$$\omega_{no} = \sqrt{2}\ 5\pi \times 10^6 \text{ rps}$$
$$\zeta_o = 0.707$$

The open loop transfer function for a 3rd order Butterworth becomes:

$$G_3(s) = \frac{2.5\pi \times 10^6}{s\left(\frac{s^2}{50\pi^2 \times 10^{12}} + \frac{s}{10\pi \times 10^6} + 1\right)} \qquad (2.2$$

The designer of the phase-locked phase modulator may consider even order Butterworth designs, using similar procedures. For example, a 4th order system requires,

$$F_4(s) = \frac{\Delta\theta_o}{NV_m}(s) = \frac{1}{\left(\frac{s^2}{\omega_n^2} + \frac{2\times 0.924}{\omega_n}s + 1\right)\left(\frac{s^2}{\omega_n^2} + \frac{2\times 0.383}{\omega_n}s + 1\right)} \qquad (2.$$

$$G_4(s) = \frac{K_v}{s\left(\frac{s}{\omega_1} + 1\right)\left(\frac{s^2}{\omega_{no}^2} + \frac{2\zeta_o}{\omega_{no}}s + 1\right)} \qquad (2.$$

$$F_4(s) = \frac{1}{\frac{s}{K_v}\left(\frac{s}{\omega_1}+1\right)\left(\frac{s^2}{\omega_{n0}^2}+\frac{2\zeta_0}{\omega_{n0}}s+1\right)+1} \qquad Eq(2.27)$$

and

$$\frac{s^4}{\omega_n^4}+\frac{2}{\omega_n^3}(0.924+0.383)s^3+\frac{2}{\omega_n^2}(1+2\times 0.924\times 0.383)s^2+\frac{2}{\omega_n}(0.924+0.383)s+1$$

$$=\frac{s^4}{K_v\omega_1\omega_{n0}^2}+\frac{1}{K_v\omega_{n0}}\left[\frac{1}{\omega_{n0}}+\frac{2\zeta_0}{\omega_1}\right]s^3+\frac{1}{K_v}\left[\frac{1}{\omega_1}+\frac{2\zeta_0}{\omega_{n0}}\right]s^2+\frac{s}{K_v}+1 \qquad Eq(2.28)$$

For the 4th order Butterworth synthesis the conditions are

$$K_v = \frac{\omega_n}{2.614} \qquad Eq(2.29)$$

$$\omega_1\omega_{n0}^2 = 2.614\,\omega_n^3 \qquad Eq(2.30)$$

$$\omega_1 = 2.614\,\omega_n - 2\zeta_0\omega_{n0} \qquad Eq(2.31)$$

$$\omega_1\omega_{n0} = \frac{\omega_{n0}+2\zeta_0\omega_1}{1.307} \qquad Eq(2.32)$$

Again limiting the amplitude frequency response to 0.1 DB over the 1.5 mcs bandwidth, the computed solution is:

For a 4th order Butterworth response at $\omega_m = 5\pi \times 10^6$ rps

$$K_v = 1.91\pi \times 10^6 = 6 \times 10^6 \text{ sec}^{-1}$$

$$\omega_1 = 23.5 \times 10^6 \text{ rps}$$

$$\omega_{no} = 8.95 \times 10^6 \text{ rps}$$

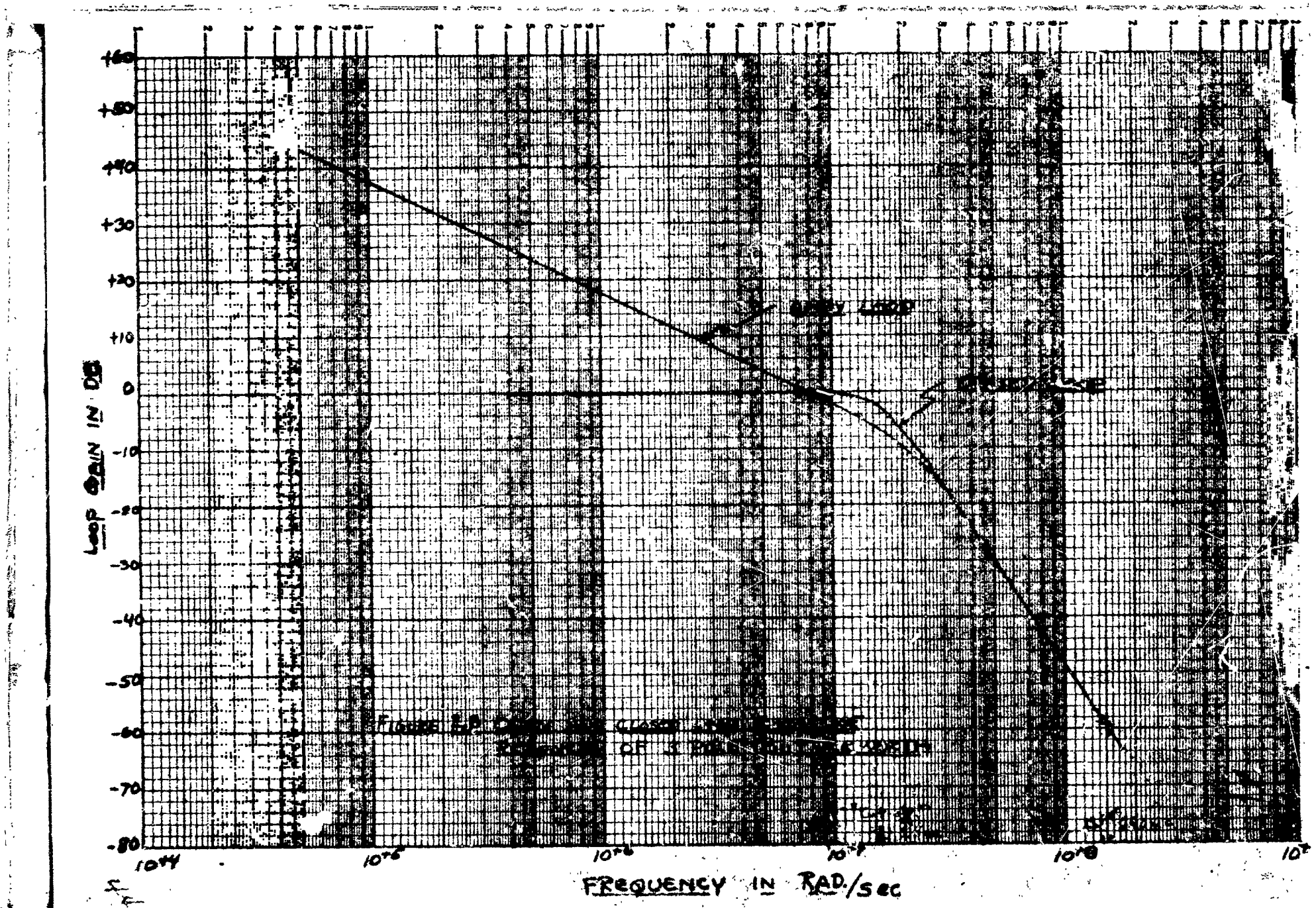
$$\zeta_o = 0.905$$

so that

$$G_4(s) = \frac{1.91\pi \times 10^6}{s\left(\frac{s}{23.5\times10^6}+1\right)\left(\frac{s^2}{80.04\times10^6}+\frac{2\times0.905}{8.95\times10^6}s+1\right)} \quad E_8(2.33)$$

The frequency responses of the 3rd and 4th order Butterworth designs were evaluated and are plotted in Figures 2.8 and 2.9.

The amplitude response Figure 2.8 of the 3rd order Butterworth shows relative attenuation of about -42 DB at 12.5 mcs and about -60 DB at 25 mcs. This is accomplished with a phase margin of 60 degrees Figure 2.10 and with a variation in group delay of about 38 nanoseconds over the 1.5 mcs bandwidth, Figure 2.11.


+60
+50
+40
+30
+20
+10
0
-10
-20
-30
-40
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-70
-80
LOOP GAIN IN DB
FREQUENCY IN RAD./SEC

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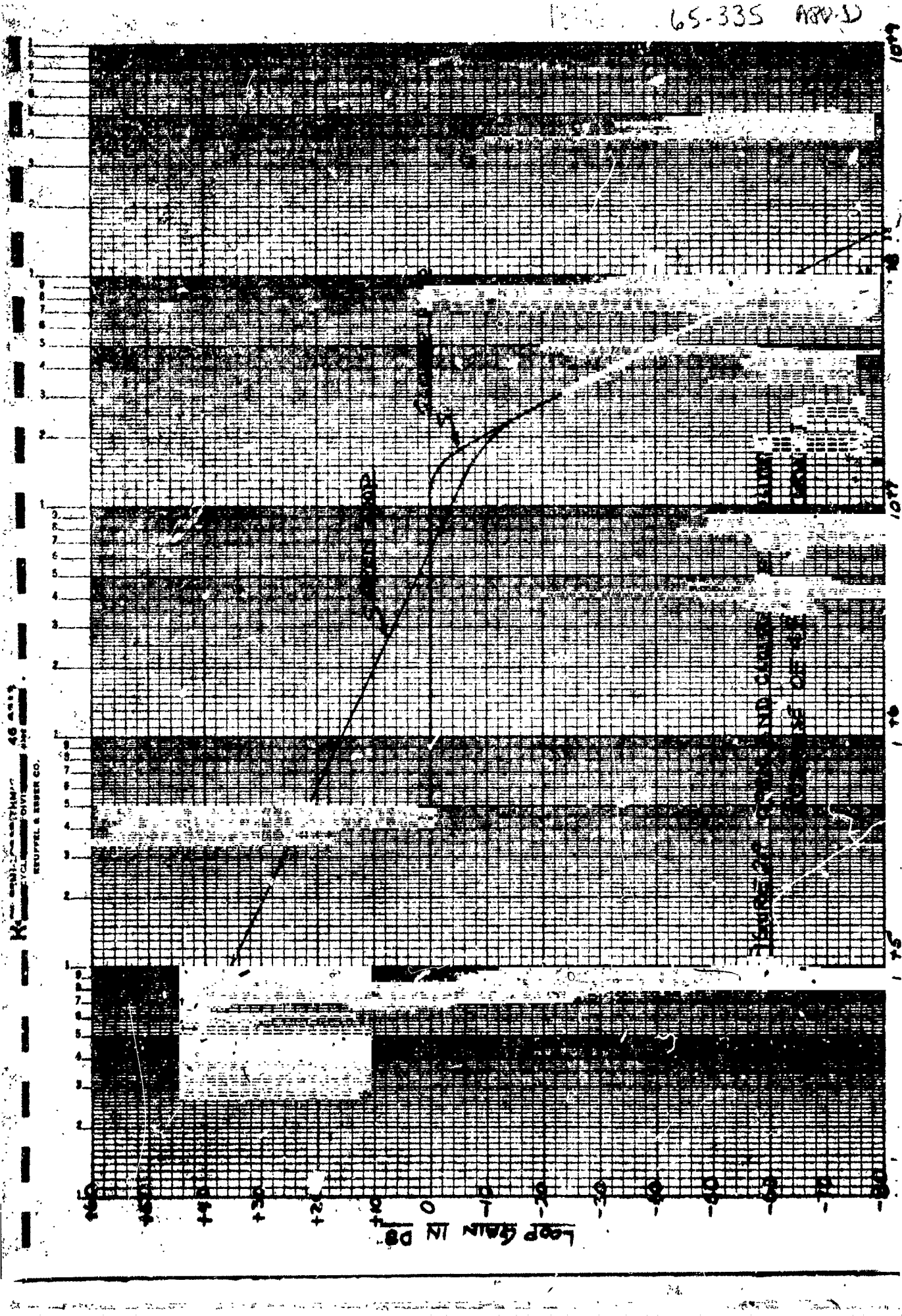

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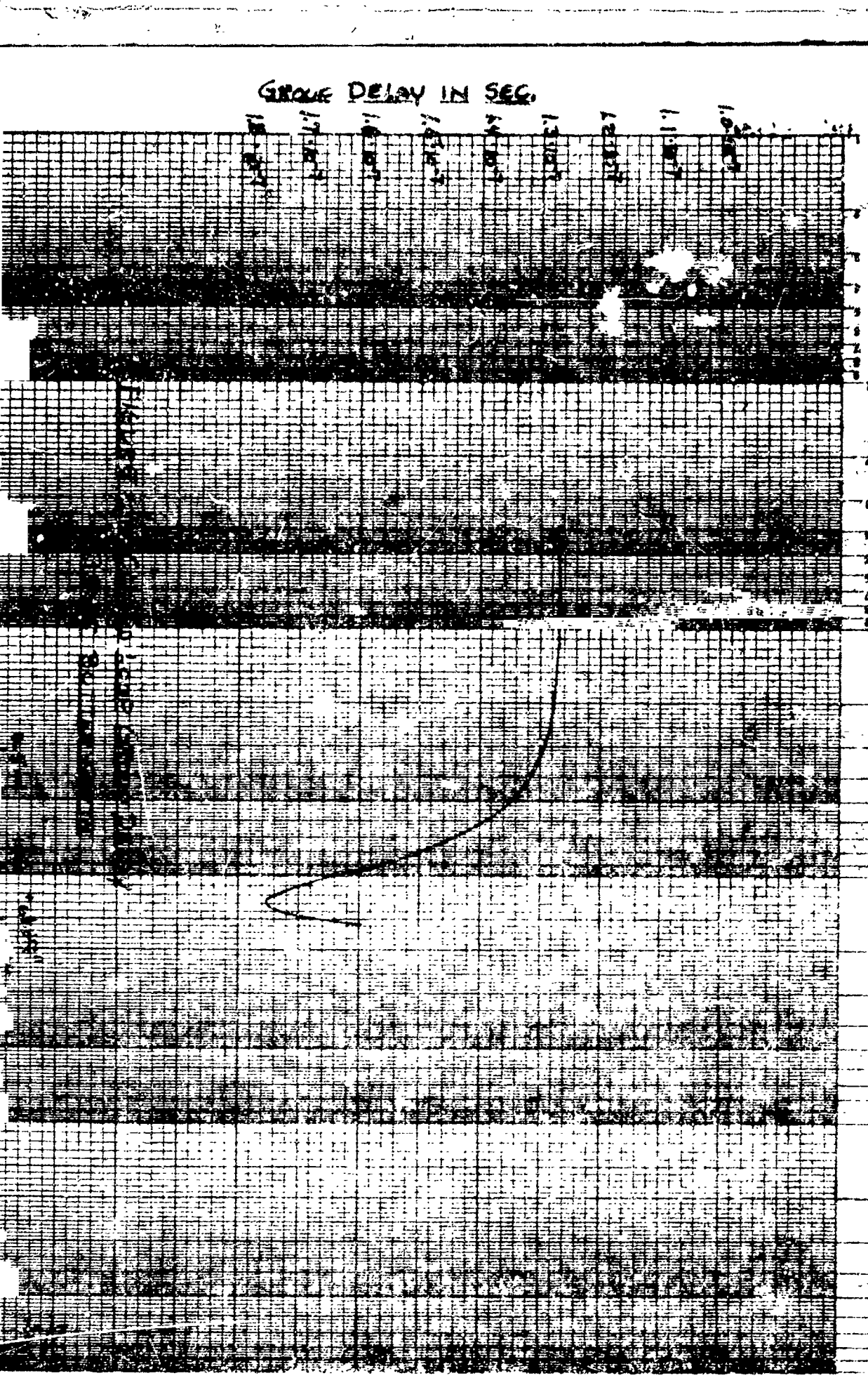
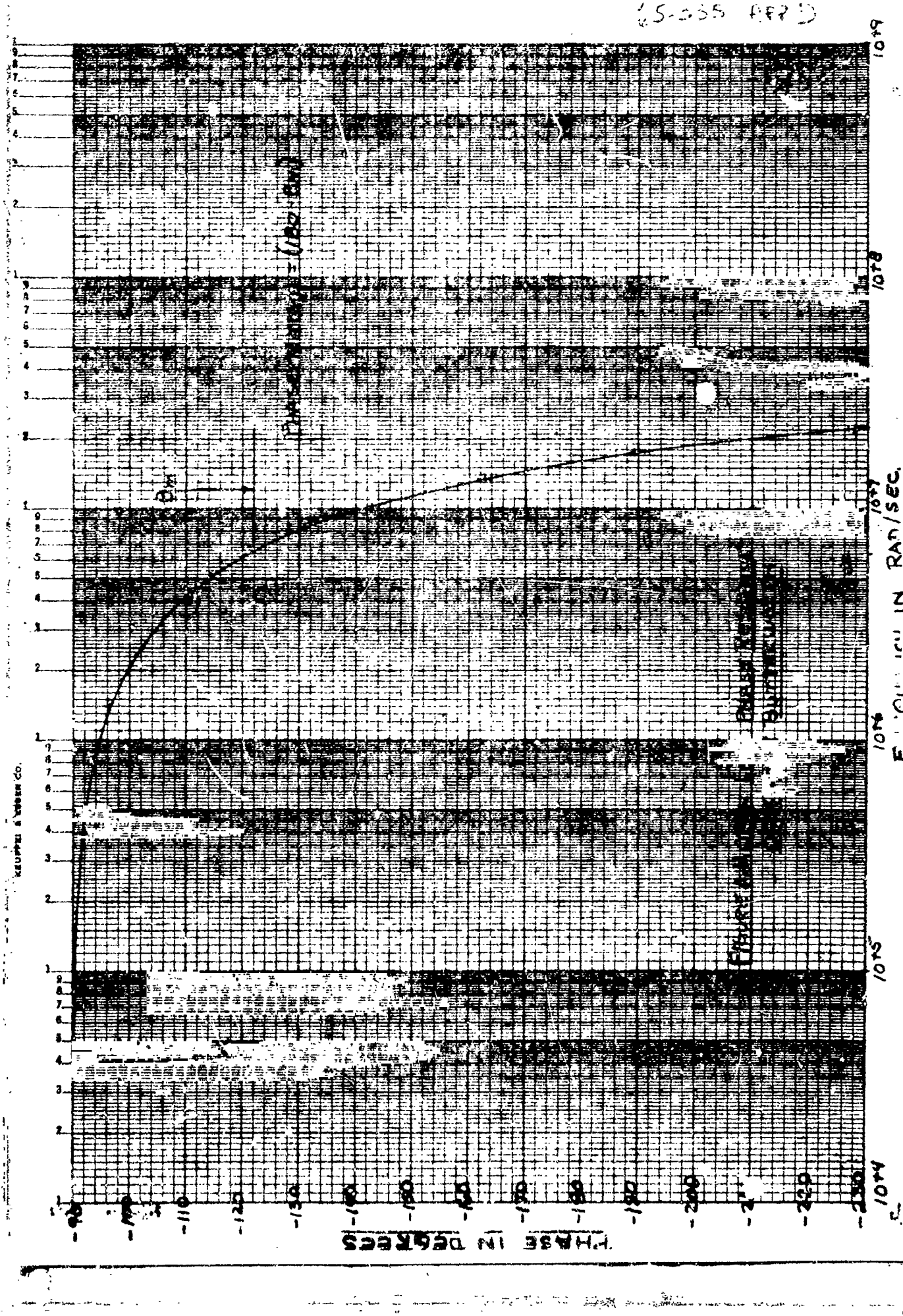
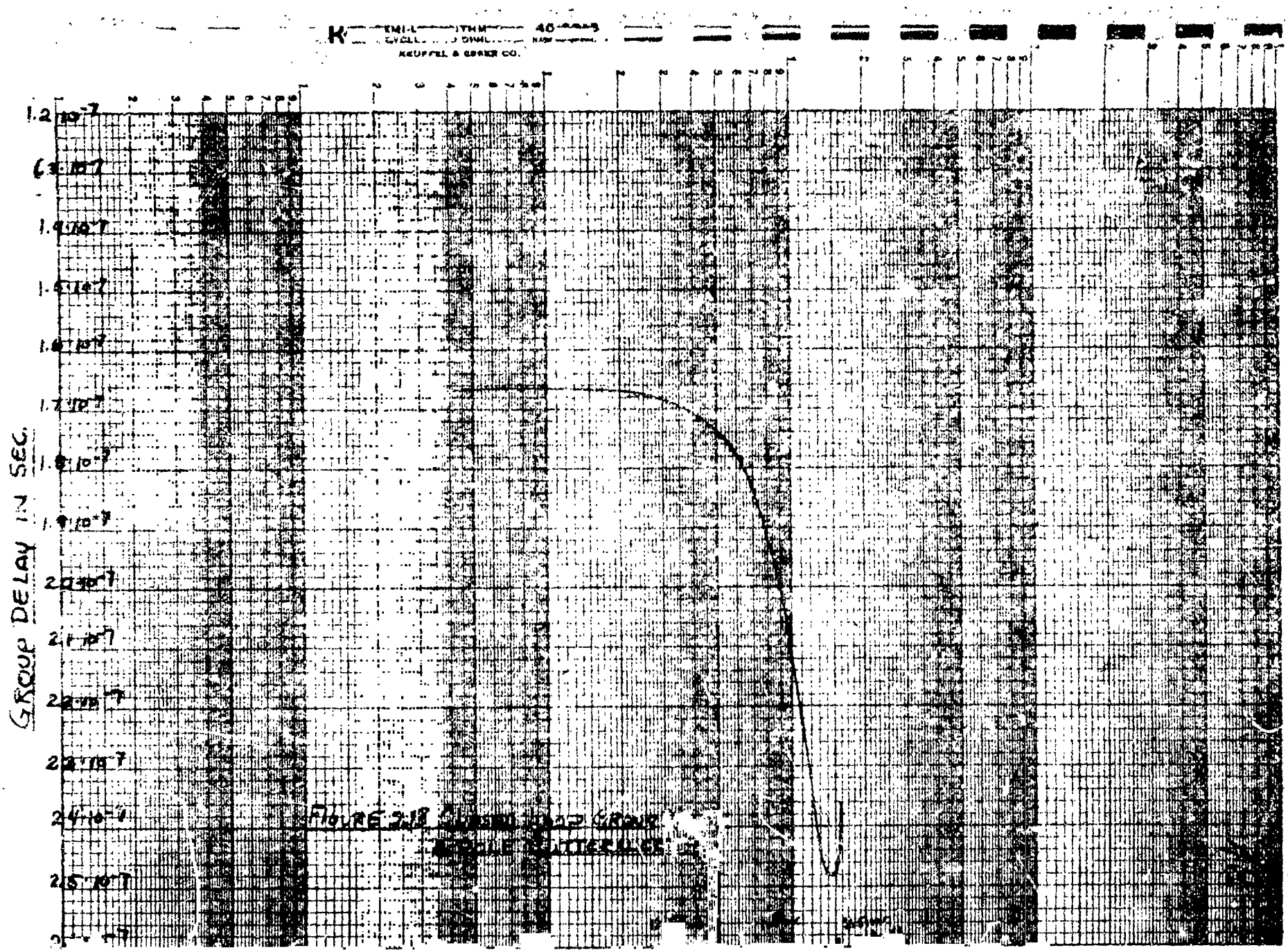

GROUP DELAY IN SEC.


PHASE IN DEGREES
FREQUENCY IN RAD/SEC.


GROUP DELAY IN SEC.

Corresponding responses of the 4th order Butterworth show relative attenuation of -56 DB at 12.5 mcs and about -[illegible]3 DB at 25 mcs, Figure 2.9. The phase margin remained at 58 degrees, Figure 2.12, while the group delay variation over the 1.5 mcs band increased to about 47 nanoseconds Figure 2.13.

3. Constant Delay Approximation: - A third design procedure which may be of greater significance for angular modulation systems of which this study is an example lies in the synthesis of a phase modulator loop having constant delay approximation. Reference to Figures (2.6) (2.11) and (2.13) for the Bode-Nichols and Butterworth procedures respectively, indicate a severe variation in the group delay vs frequency responses particularly in the top of the modulation band. For some system the indicated variation may produce delay distortion of serious consequences. In the design of the phase modulator, greater emphasis may be placed on the delay response than has been afforded by either the Bode-Nichols or Butterworth procedures.

A design procedure similar to that developed above for the Butterworth maximally flat amplitude response may also be developed for linear phase (or constant delay) vs frequency approximation. For constant delay approximation the poles of the closed loop phase-locked modulator are forced to assume a uniform distribution along a line in the left half plane

parallel to the imaginary axis as illustrated in Figure (2.14).

A three pole distribution approximating constant delay is described by a closed loop phase modulator transfer function:

$$F_3(s) = \frac{\Delta\theta_o}{N V_M}(s) = \frac{1}{\left(\frac{s}{\sigma}+1\right)\left(\frac{s^2}{\sigma^2+b^2} + \frac{2\sigma}{\sigma^2+b^2}s + 1\right)} \qquad \text{Eq (2.34)}$$

The form of the open loop transfer function, as in the case of the Butterworth design is

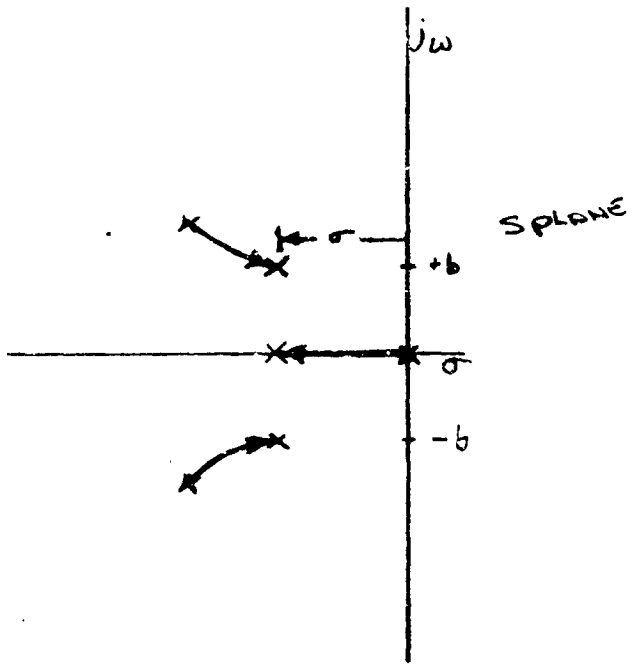
$$G_3(s) = \frac{K_v}{s\left(\frac{s^2}{\omega_{no}^2} + \frac{2\zeta_o s}{\omega_{no}} + 1\right)} \qquad \text{Eq (2.35)}$$

In terms of the open loop parameters the closed loop function is

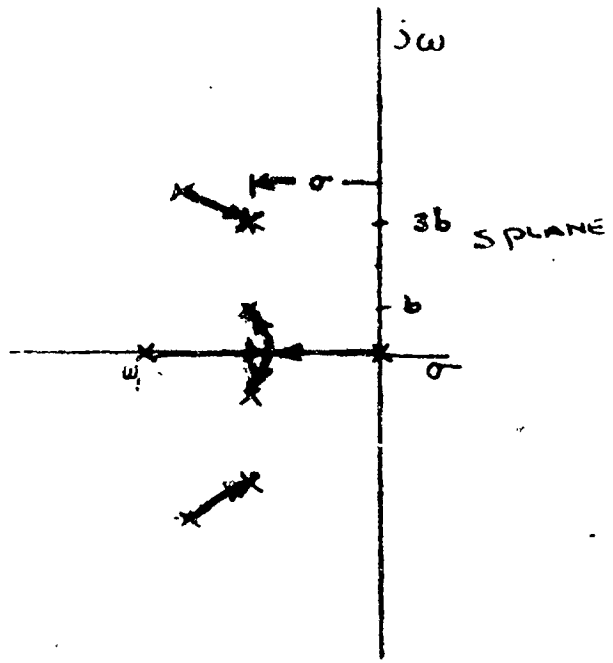
$$F_3(s) = \frac{1}{\frac{s}{K_v}\left(\frac{s^2}{\omega_{no}^2} + \frac{2\zeta_o}{\omega_{no}}s + 1\right) + 1} \qquad \text{Eq (2.36)}$$

and the condition for synthesis of approximate constant delay is expressed by the equality:

$$\frac{s^3}{\sigma(\sigma^2+b^2)} + \frac{3s^2}{\sigma^2+b^2} + \frac{3\sigma^2+b^2}{\sigma(\sigma^2+b^2)}s + 1 = \frac{s^3}{K_v\omega_{no}^2} + \frac{2\zeta_o s^2}{K_v\omega_{no}} + \frac{s}{K_v} + 1 \qquad \text{Eq (2.37)}$$



(a) 3 pole Approximation



(b) 4 pole Approximation

Fig 2.14 Constant Delay Phase Lock Phase Modulator Approximation - Root Locus

Therefore the open loop parameters, for a specified closed loop distribution of poles are:

$$K_v = \frac{\sigma(\sigma^2 + b^2)}{3\sigma^2 + b^2} \qquad \text{Eq (2.38)}$$

$$\omega_{no} = \sqrt{3\sigma^2 + b^2} \qquad \text{Eq (2.39)}$$

$$\zeta_o = \frac{3\sigma}{2}\sqrt{\frac{1}{3\sigma^2 + b^2}} \qquad \text{Eq (2.40)}$$

The open loop transfer function now becomes:

$$G_o(s) = \frac{\dfrac{\sigma(\sigma^2 + b^2)}{3\sigma^2 + b^2}}{s\left(\dfrac{s^2}{3\sigma^2 + b^2} + \dfrac{3\sigma}{3\sigma^2 + b^2}s + 1\right)} \qquad \text{Eq. (2.41)}$$

where the roots are at

$$s = 0$$
$$s = \frac{3\sigma}{2} + j\frac{\sqrt{3\sigma^2 + 4b^2}}{2}$$
$$s = \frac{3\sigma}{2} - j\frac{\sqrt{3\sigma^2 + 4b^2}}{2} \qquad \text{Eq (2.42)}$$

As the Butterworth design may be extended to 4th and higher order functions, so also may the synthesis of higher order

constant delay approximations. For a 4th order delay approximation Fig. (2.14b), the synthesis requires open loop parameters satisfying the following conditions:

$$K_v = \frac{(\sigma^2+b^2)(\sigma^2+9b^2)}{4\sigma(\sigma^2+5b^2)} \qquad \text{Eq (2.43)}$$

$$\omega_1 = \frac{4\sigma(\sigma^2+5b^2)}{\omega_{no}^2} \qquad \text{Eq (2.44)}$$

$$\zeta = \frac{\omega_{no}(6\sigma^2+10b^2-\omega_{no}^2)}{8\sigma(\sigma^2+5b^2)} \qquad \text{Eq (2.45)}$$

$$\omega_{no}^6 - 2(3\sigma^2+5b^2)\omega_{no}^4 + 16\sigma^2(\sigma^2+5b^2)\omega_{no}^2 - 16\sigma^2(\sigma^2+5b^2)^2 = 0 \qquad \text{Eq (2.46)}$$

Design with Bessel Polynomials for Maximally Flat Delay Response: -

As an alternative to the linear distribution of poles as required in Fig. 2.14 (which gives constant delay with a ripple factor), Bessel polynomials may be selected for a maximally flat delay response. Derivation of the Bessel polynomials is described in the technical literature. A convenient table of coefficients for the polynomials in (s) are given, for example, in Weinberg, Louis, "Modern Synthesis Network Design from Tables, Part III", Electronic Design, Oct. 15, 1956. This table is repeated here in Fig. 2.15.

From the normalized values given in Fig. 2.15 the following distributions of poles are required to synthesize the Bessel polynomials:

For a 3rd order Bessel $F_3(s)$:

$$s = -2.32219$$
$$s = -1.83891 + j\ 1.75438 \qquad \text{Eq (2.47)}$$
$$s = -1.83891 - j\ 1.75438$$

For a 4th order Bessel $F_4(s)$:

$$s = -2.89621 + j\ 3.67234$$
$$s = -2.89621 - j\ 3.67234 \qquad \text{Eq (2.48)}$$
$$s = -2.10379 + j\ 2.65742$$
$$s = -2.10379 - j\ 2.65742$$

Table III - 2

Element Values (in ohms, henrys, farads) of a Maximally-Flat Time-Delay Network with Resistance Termination at Load End ($R_1 = 1$ for all values of n). (For this case unprimed values correspond to a current-source input for n odd and to a voltage-source input for n even.)

Value of n	C_1 or L_1'	L_2 or C_2'	C_3 or L_3'	L_4 or C_4'	C_5 or L_5'	L_6 or C_6'	C_7 or L_7'	L_8 or C_8'	C_9 or L_9'	L_{10} or C_{10}	C_{11} or L_{11}'
1	1.0000										
2	0.3333	1.0000									
3	0.1667	0.4800	0.8333								
4	0.1000	0.2899	0.4687	0.7181							
5	0.0667	0.1948	0.3103	0.4218	0.6231						
6	0.0476	0.1400	0.2246	0.3005	0.3821	0.5595					
7	0.0357	0.1055	0.1704	0.2288	0.2827	0.3487	0.5111				
8	0.0278	0.0823	0.1338	0.1806	0.2227	0.2639	0.3212	0.4732			
9	0.0222	0.0660	0.1077	0.1463	0.1811	0.2129	0.2465	0.2986	0.4424		
10	0.0182	0.0541	0.0886	0.1209	0.1549	0.1880	0.2037	0.2389	0.2712	0.4161	
11	0.0152	0.0451	0.0741	0.1016	0.1369	0.1499	0.1708	0.. 16	0.2175	0.2639	0.3958

Table III-3

Exact Coefficients of the Polynomials $h_n(s) = s^n + a_{n-1}s^{n-1} + a_{n-2}s^{n-2} + \ldots + a_1 s + a_0$ Used for Maximally-Flat Time-Delay Networks

n	a_0	a_1	a_2	a_3	a_4	a_5	a_6	a_7	a_8	a_9	a_{10}
1	1										
2	3	3									
3	15	15	6								
4	105	105	45	10							
5	945	945	420	105	15						
6	10,395	10,395	4,725	1,260	210	21					
7	135,135	135,135	62,370	17,325	3,150	378	28				
8	2,027,025	2,027,025	945,945	270,270	51,975	6,930	630	36			
9	34,459,425	34,459,425	16,216,200	4,729,725	945,945	135,135	13,860	990	45		
10	654,729,075	654,729,075	310,134,825	91,891,800	18,918,900	2,837,835	315,315	25,740	1,485	55	
11	13,749,310,575	13,749,310,575	6,547,290,750	1,964,187,225	413,513,100	64,324,260	7,567,560	675,675	45,045	2,145	66

Table III-4 Zeros of Polynomials $h_n(s) = s^n y_n(1/s)$ Derived from the Bessel Polynomials for Values of n from 1 through 11

n	Zeros
1	-1.0000000
2	-1.5000000 ±j0.8660254
3	-2.3221854; -1.8389073 ±j1.7543810
4	-2.8962106 ±j0.8672341; -2.1037894 ±j2.6974180
5	-3.6467386; -2.3519564 ±j1.7426614; -2.3246743 ±j3.5710229
6	-4.2483594 ±j0.8675097; -3.7357084 ±j2.6262723; -2.5139322 ±j4.4926730
7	-4.9717868; -4.7584905 ±j1.7392861; -4.0701392 ±j3.5171740; -2.6856769 ±j5.4206941
8	-5.7439860 ±j0.8676144; -5.2189860 ±j2.6539115; -4.3662892 ±j4.4144425; -2.9208488 ±j6.4161751
9	-6.2970193; -6.1293679 ±j1.7378484; -5.6044218 ±j3.4981573; -4.6384399 ±j5.3178717; -3.0793608 ±j7.4914639
10	-6.9820449 ±j0.8674691; -6.4683162 ±j2.6326995; -6.1532916 ±j4.4113683; -5.3678282 ±j6.3694471; -3.4862195 ±j8.5249858
11	-7.6283398; -7.3813378 ±j3.5761917; -6.1156483 ±j7.1370208; -7.4642299 ±j1.7370208; -7.0878934 ±j5.4890148; -3.8297231 ±j9.5771116

Fig 2.15 Tables for Maximally Flat Delay Synthesis - Normalized values (From Weinberg, L.)

The synthesis of the PLC phase modulator for these closed loop Bessel characteristics requires a distribution of poles in the open loop transfer function as fcllows:

For a 3rd Order Bessel $G_3(s)$

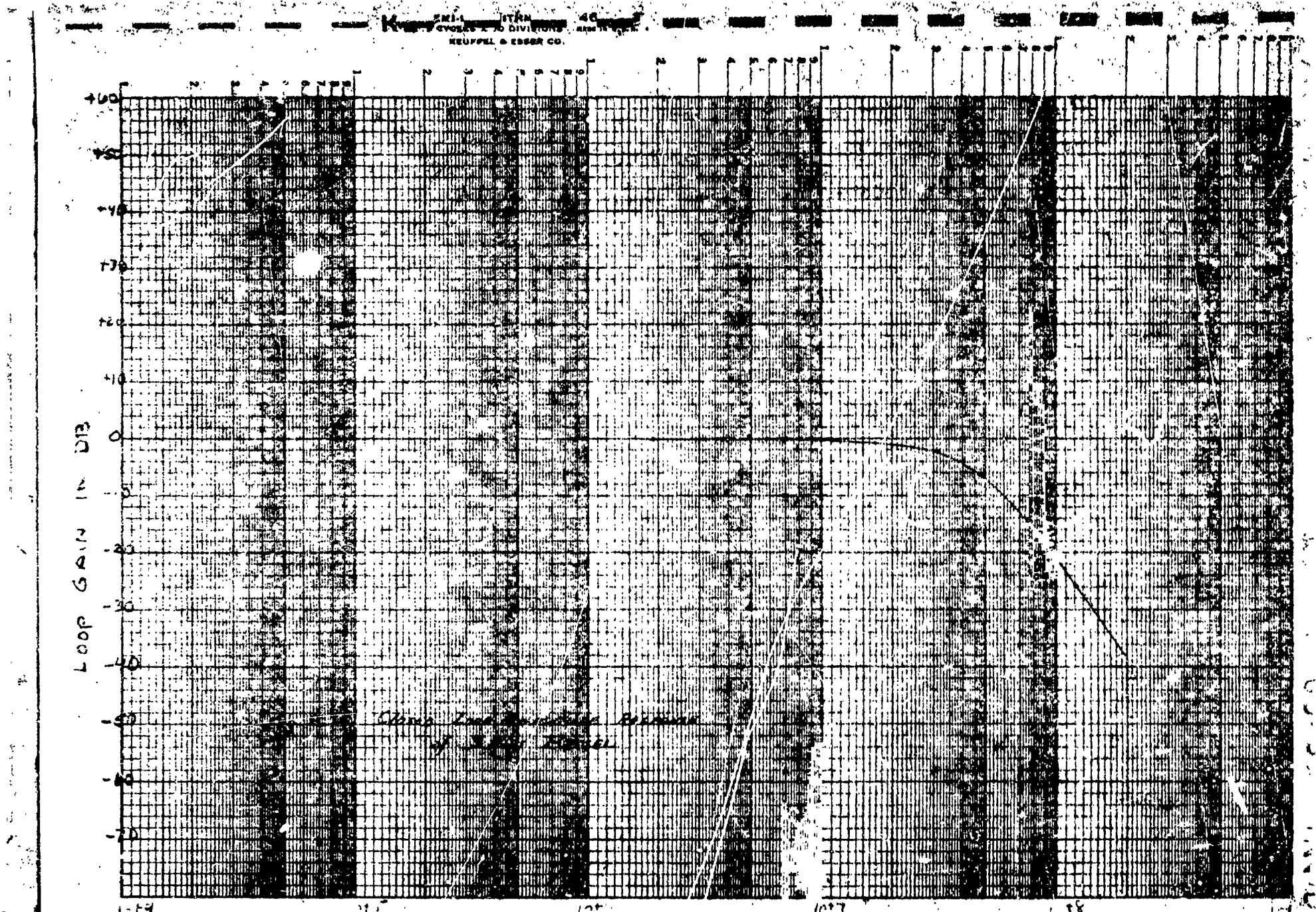
$$s = 0$$
$$s = -3.00000 + j\ 2.44949 \qquad \text{Eq (2.49)}$$
$$s = -3.00000 - j\ 2.44949$$

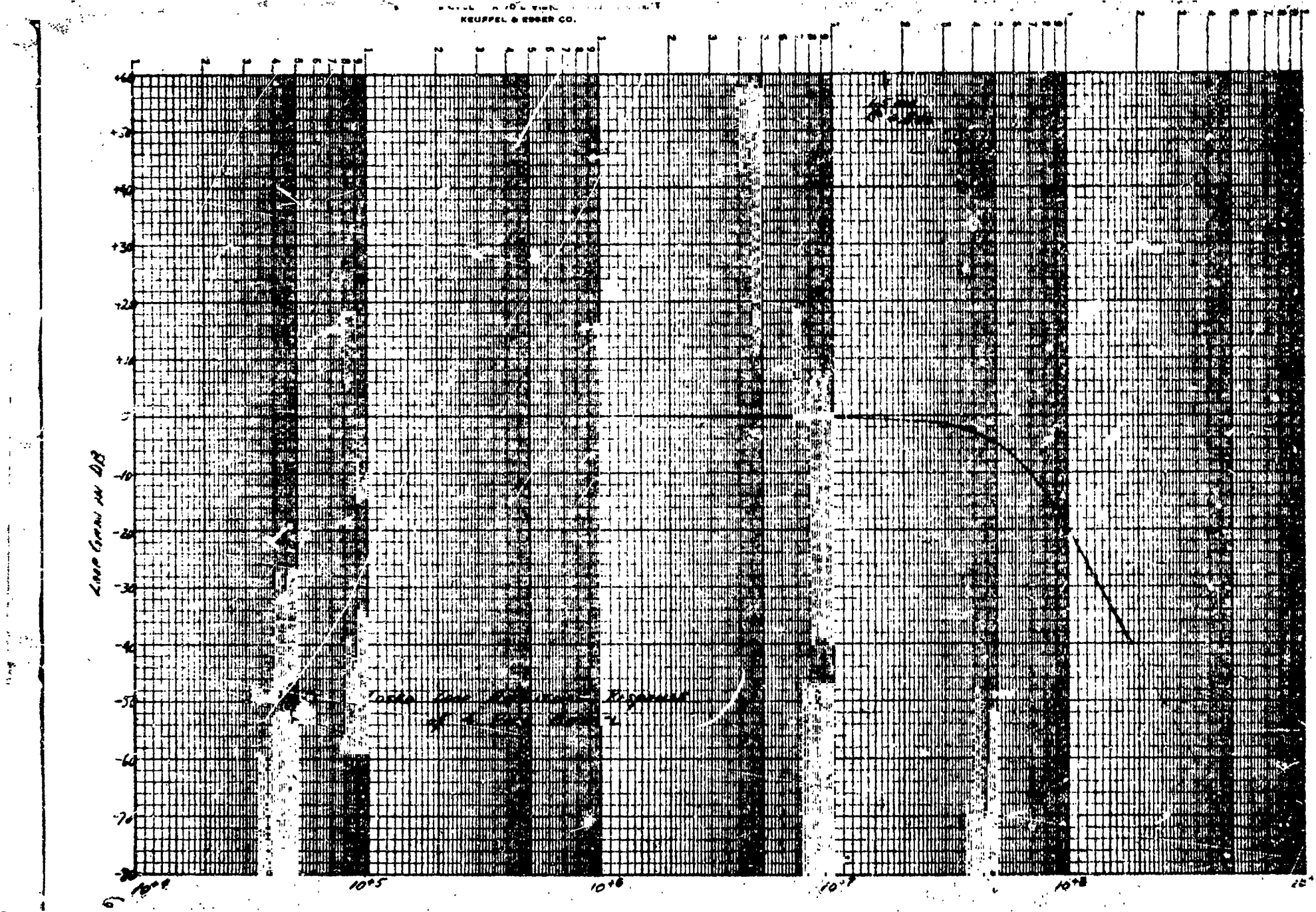
For a 4th Order Bessel $G_4(s)$

$$s = 0$$
$$s = -5.23548 \qquad \text{Eq (2.50)}$$
$$s = -2.38226 + j\ 3.79214$$
$$s = -2.38226 - j\ 3.79214$$

Using the digital computer, these parameterr were used to obtain data for curves of Amplitude and delay vs frequency. In order to compare the Bessel and Butterworth designs, the Bessel responses were normalized to give a -0.2db variation of amplitude frequency response at 1.5mcs. The amplitude responses are Gaussian in shape. They are given in Figures (2.16) and (2.17) for the 3rd and 4th order Besuels, respectively.

The time delay responses for the same normalization are given in


KEUFFEL & ESSER CO.
+60
+40
+30
+20
+10
0
-10
-20
-30
-40
-50
-60
-70
LOOP GAIN IN DB


KEUFFEL & ESSER CO.
+40
+30
+20
+10
0
-10
-20
-30
-40
-50
-60
-70
-80
Loop Gain in DB
10^{+4}
10^{+5}
10^{+6}
10^{+7}
10^{+8}

Figures (2.18) and (2.19). In either 3rd or 4th order Bessel designs note that the variation of group delay is extremely small (<1 nanosecond over the band to 1.5mcs) to frequencies much higher than 1.5mcs. Thus intermodulation due to delay distortion is vastly improved over the Bode-Nichols and Butterworth designs.

4. Comparative Evaluation of Design Procedures: - In the study reported herein an attempt has been made to apply some of the more familiar synthesi techniques to the design of a PLC phase modulator. The designs were representative but not all-indusive. The ingenious designer may certainly visualize other pole distributions capable of good results, especially if a compromise between delay and amplitude responses is required or justified.

At this point a listing of the significant features, advantages and disadvantages of the design procedures studied in this investigation is offered to develop a preferred technique for the mechanization phase.

(A) Synthesis using Bode-Nichol's Diagrams:

1. The procedure is primarily graphical, using asymptotic curves

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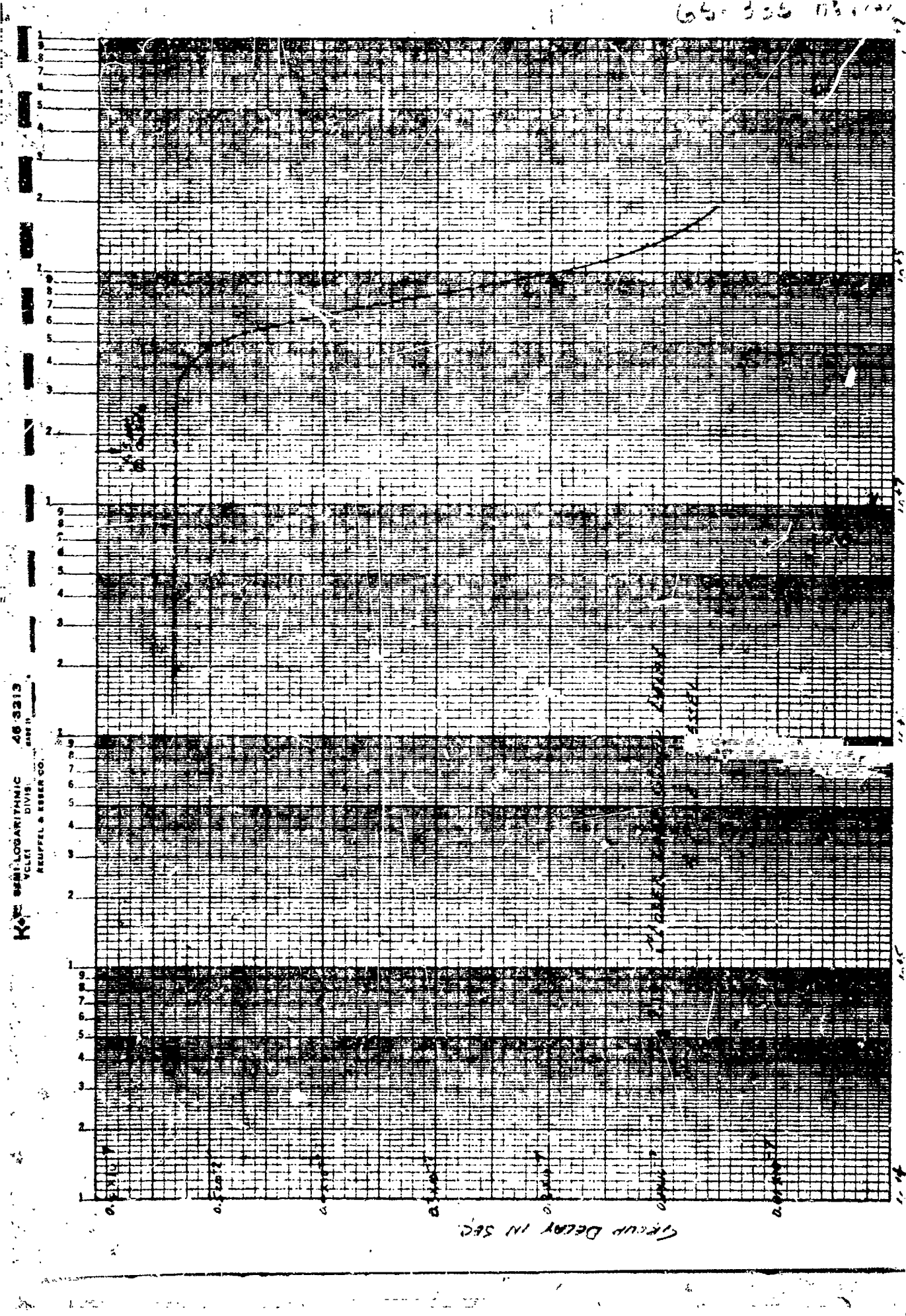
Circuit Delay in sec

in the Bode diagram, and M_p contours of constant magnitude in the Nichol's chart.

2. The procedure is very rapid and easy to use, particularily for systems possessing real roots, although it is slightly more difficult to use with complex roots.

3. Excellent results are possible in synthesis for a specified amplitude vs frequency response.

4. Rather poor results are anticipated in synthesis of a specified closed loop delay vs frequency response. This is the primary disadvantage when used with angular modulation systems.

5. The procedure does permit a simple and excellent graphical illustration of stability margins of the design.

6. The procedure also permits a simple graphical illustration of transport lag effects on the system performance. It is in this respect that the Nichol's chart may supplement the computation necessary for Butterworth or Bessel synthesis procedures.

(B.) Synthesis using Butterworth Pole Distributions:

1. The procedure is primarily computational although a root locus diagram is useful for illustrative purposes.

2. The procedure gives a maximally flat system amplitude response over the inband spectrum. It gives excellent out of band rejection depending upon the permissible inband amplitude ripple.

3. The procedure gives a poor system delay response. A large variation in group delay occurs near the top of the inband spectrum. As with the Bode-Nichol's method this is the primary disadvantage of the method. Large delay distortion intermodulation products will occur in the system output.

4. The procedure is not easily adaptable to account for amplitude peaking caused by transport lag effects.

(c) Synthesis using Constant Delay Pole Distributions:

1. The procedure is primarily computational in its application, although here a root locus is useful for illustrative purposes.

2. Synthesis of Bessel polynomials gives a maximally flat system delay vs frequency response over the in-band spectrum. (The linear pole distribution gives a constant delay approximation with a ripple factor). This is a primary advantage for angular modulation systems.

3. The Bessel synthesis results in poor out-of-band rejection, the amplitude response following a Gaussian curve (for a large number of poles).

4. As with the Butterworth synthesis, similar difficulty is encountered in accounting for amplitude peaking effects caused by transport lag effects. But since the Bessel amplitude response is falling off more rapidly within the in-band spectrum than is the case for the Butterworth designs, some peaking near the top of the modulation band may actually be beneficial to the frequency response of the Bessel design. The effect of transport lag can probably best be shown by supplementing the design with the Nichols graphical chart.

In conclusion, with respect to synthesis procedures, the studies reported herein reveal that rather remarkable results have been shown to be theoretically possible, considering the inherent constraints imposed by the fundamental characteristics of phase locked loops. For angular modulation (PM) applications:

(a) the necessary emphasis on delay vs frequency response to prevent delay distortion and intermodulation, requires a Bessel synthesis, or at least a constant delay approximation in the PLC design, and

(b) if necessary, phase linear amplitude equalization should be applied outside the PLC loop to shape the overall system response.

5. Equalization Concepts: - The characteristics and performance of the possible PLC phase modulator designs achieved by the above procedures may in some cases be significantly improved by equalization networks placed outside the PLC loop. In order to achieve optimum amplitude and phase (or delay) vs frequency responses simultaneously many mathematical models might be envisioned. But practical economics of design plus loop stability requirements limit the synthesis of poles to three or four as illustrated above. With a four pole design the loop would be limited to its inherent pole at zero, plus a real axis pole at some high frequency W_1, and a complex conjugate pair at a relatively high resonant frequency W_n.

Thus in order to improve performance of the illustrated designs (which are not suggested to foreclose other possible distributions of poles of the closed-loop transfer function) it may be necessary to adjust the overall modulator response either by pre-emphasis to the modulating spectrum or by post-modulation compensation to the VCO output wave. In either case the external network would not be a direct factor in the design of the PLC loop

for stability.

For example if the modulation signal consists of an ensemble of discrete tones or channels, as perhaps in a telemetry and sidetone ranging system, it would be a simple matter to adjust for variations from ideal frequency (amplitude) response by weighting the individual tones prior to the signal combiner. Pre-emphasis filters should not ordinarily be used without due consideration of their effect on phase as well as amplitude response.

The use of premodulation delay equalization using all-pass first order lattice networks or equivalents in order to compensate for the peaking in the delay responses of Figures (2,6) and (2,13) is theoretically possible. It is believed that better results might be obtained with second order all-pass structures placed in the 50 MC output channel of the VCO outside the PLC loop.

Should it be desired to synthesize a constant delay approximation network of a large number of poles, greater than 4, it is suggested that this may be accomplished by using all-pass structures following the

VCO. Admitting symmetrical complex conjugate zeroes in the right half plane the distribution of roots may be arranged in patterns such as shown in Figure (2.20).

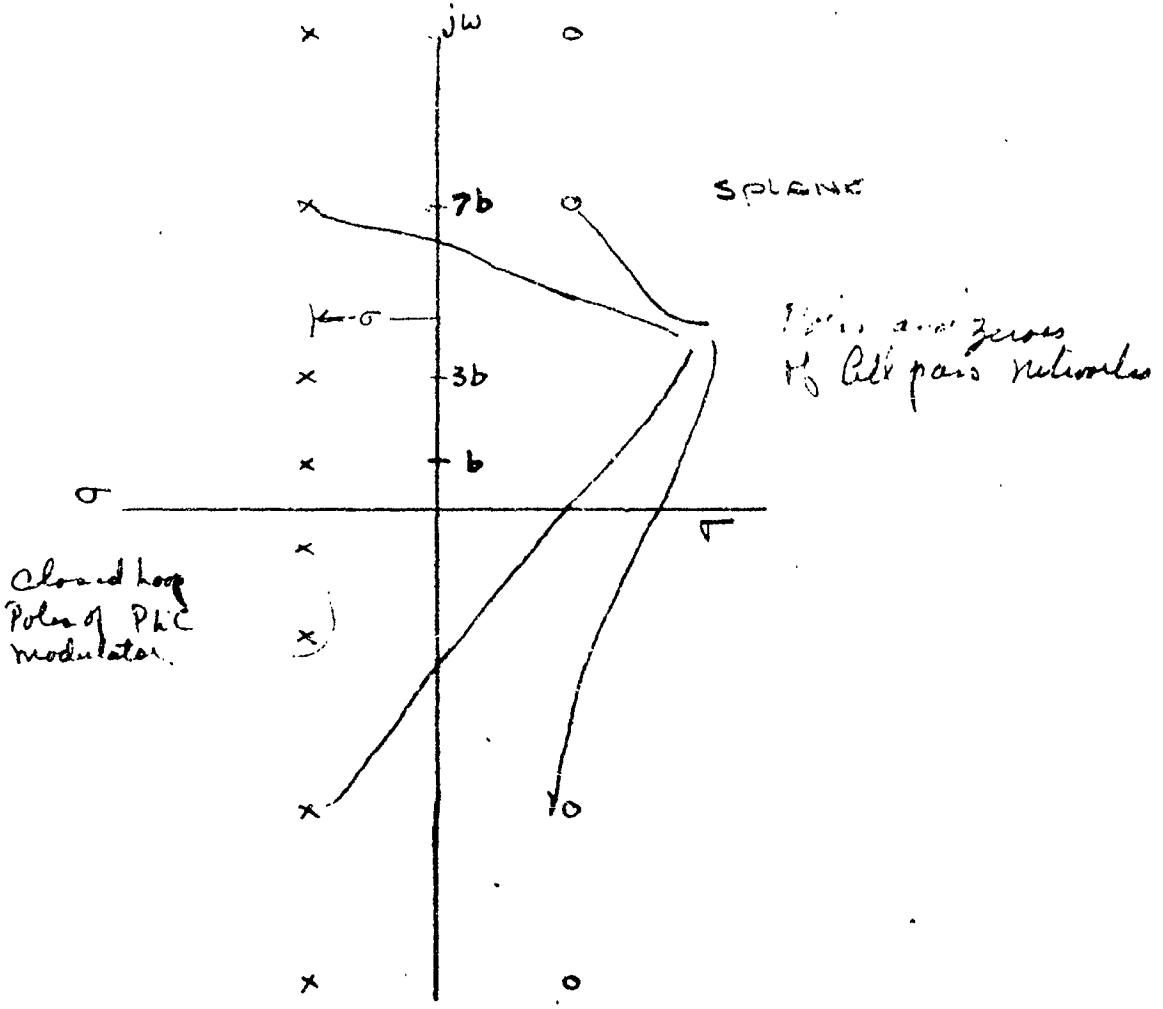

Fig 2.20 Constant delay approximation of PLC phase modulator with Post modulation

Since the all-pass network contributes twice the phase angle of the complex pair in the left half plane, the distribution must be nonuniform as shown in the sketch.

2. Evaluation and Recommendations: - The designer must consider that A PLC phase modulator operating at bandwidths in the megacycle regions must have an equivalent mathematical model, f (s), with poles of the (open) loop characteristic equation including at least the following:

$S = 0$ -- inherent in all Phase locked circuits.

$S = W_1$ -- inherent in the VCO control.

$S = -\sigma \pm j\,w$ -- desired for filtering of phase detector harmonics of mixing and for loop bandwidth shaping.

Thus, the design must be based upon the synthesis of an ideal distribution of these poles in the complex frequency plane to achieve the fidelity required over the desired range of input signals. Section IV below describing implementation of circuits, suggests methods of achieving a fourth order

system. In the distribution of these poles in the closed loop mode, it is clear that high fidelity angular modulation systems require constant delay vs frequency characteristics to avoid intermodulation of an ensemble of signals, and thus the Bessel distribution is preferred. But if the 4 pole Bessel is selected, what are the consequences on frequency response and out-of-band rejection of undesired signals generated by the feedback divider and plane detector circuitry?

To conduct a comparative analysis of the Butterworth and Bessel designs the curves of Figures (2.8), (2.9) (2.17), and (2.19) were computed all at a maximum droop of -0.2 db at the top frequency of 1.5 mcs. For this condition comparison of the 4th order amplitude responses of the Butterworth, Figure (2.9), and the Bessel, Figure (2.19), curves reveals superior out-of-band rejection at 12.5 and 25 mcs in the Butterworth design as compared to the Bessel response:

frequency	4 pole Butterworth	4 pole Bessel
1.5 mcs	-----0.2 db	-----0.2 db
12.5 mcs	----- 56 db	----- 13 db
25 mcs	----- 79 db	----- 34 db

One is to be remirded however, that the specification for the phase modulator requires an amplitude frequency response of ± 0.5 db at 1.5 mcs. This specification may be interpreted to mean that the peak to peak variation permissible over the modulation band from 0 to 1.5 mcs is a total of 1 db. Assuming that one-half (0.5 db) of this can be logically allotted to the phase modulator the whole design may be frequency scaled accordingly:

frequency	4 pole Bessel
1.5 mcs	-----0.5 db
12.5 mcs	----30.5 db
25. mcs	----51.5 db

From the normalized data computed for the Bessel distribution under the frequency scaling for - 0.5 db at 1.5 mcs, the delay variation remains

well within the tentative objective of less than one nanosecond.

The conclusion can be drawn that it is possible to synthesize a PLC phase modulator having a Bessel distribution of poles with an extremely linear delay variation characteristic, and a satisfactory amplitude response. This assumes that the phase detector is designed for a fundamental harmonic V_H at 25 mcs and that sufficient balance is obtained to prevent 1.5 mcs feedthrough at a level greater than -20 db relative to the sensitivity of the peak modulating signal V_M.

The closed loop parameters to be synthesized for a Bessel distribution giving -0.5 db loss at 1.5 mcs become $F_4(s)$

$$S = -2.72243 \pm j0.815199 \times 10^7$$

$$S = -1.97756 \pm j2.49795 \times 10^7 \qquad \text{Equation (2.51)}$$

To synthesize these values the open loop parameters are:

$G_4(s)$

$$S = 0$$

$$S = -4.92135 \times 10^7$$

$$S = -2.23932 \pm j\,3.56461 \times 10^7 \qquad \text{Equation (2.52)}$$

From these values

$$W_{no} \approx 42 \times 10^6 \text{ rps.}$$

$$S_o \approx 0.53$$

$$K_v \approx 9.5 \times 10^6$$

III. PRACTICAL PROBLEMS IN MECHANIZATION

In this section, a description of the requirements imposed upon the major subcircuits is presented. The guiding theme has been to avoid generation of intermodulation and distortion is so far as is practical, rather than to emphasize compensation after the fact.

A. Feedback Divider: - The specification requires a wide peak phase deviation of the output PM signal of ± 4 radians which is far in excess of the range of realizable phase detectors. The desired deviation is possible only if a frequency divider is utilized in the feedback channel for the purpose of compressing the phase deviation to a lower peak value which does fall within the linear range of the detector. The magnitude of the division ratio must be determined.

It might be suggested that a very large ratio be used to enable the use of a simple product (or sinusoidal) type phase detector having linearity over only a few degrees. This suggestion is, however, a pitfall to be avoided.

In selecting a value for N (the divider ratio) the following points are emphasized:

1. Although a large value of N might be used, it is impossible to compress the signal bandwidth (at the detector) to less than a first order spectrum, i.e., 0 to 1.5 mcs in this application, and
2. Large (or even modest) values of N operating on a broadband modulation on a relatively low carrier frequency results in bringing the sum or ac term (at 2 w_r) of the phase detector output sufficiently close to the modulation spectrum that an ideal filter to reject the harmonic (and the carrier feedthrough) can no longer be automatically assumed. Suppression of the harmonic component becomes increasingly difficult as the divider ratio N is increased.

Consideration of these factors plus the practical problems involved in the design of a linearized phase detector lead us to the conclusion that a feedback divider ratio of value N = 4 is most desirable from all aspects. With N = 4 the peak deviation of 4 radians is compressed to 1 radian at a carrier frequency of 12.5 mcs. This is a suitable carrier frequency at which to construct the phase detector using conventional techniques. It permits significant suppression of the carrier and harmonic outputs of the phase detector by simple lag filtering within the phase modulator loop.

B. Linearity Considerations: - The linearity of the components within the PLC phase modulator is important in satisfying the required fidelity specificat But since one of the primary purposes of using feedback is to improve linearity, we shall examine the compensatory influency of the loop on phase detector and VCO nonlinearities, using the Bode-Nichols design as a typical loop configuration.

1. Significance of Two-tone Detector and VCO Analysis: - In the paragraphs below, considerable space is given to two-tone analysis of the phase detector and the VCO. It is our purpose to describe at this point the effects of the control loop upon the intermodulation spectra produced by the nonlinearities of the Detector and VCO.

In the literature on nonlinear feedback control theory serious deficiencies are observed in the techniques for estimating performance in the presence of multitoned signals. Neither the describing function technique nor the method of Booton (Booton, R. D., "Analysis of Nonlinear Control Systems with Random Inputs," Proceedings of the Nonlinear Circuit Analysis Symposium, April 24, 1953 PP369-392,) which is currently being adopted in the analysis of phase locked loops is completely satisfactory for computation of intermodulation between tones. The problem faced in the PLC - Phase Modulator is complicated beyond the usual systems in that two major nonlinearities are cascaded within the loop rather than the usual single non-

linearity. As a consequence, a direct and accurate computation of the intermodulation measurable in a two tone test is presently beyond the scope of mathematical art.

In lieu of a suitable mathematical design tool for handling cascaded nonlinearities (phase detector and VCO) in the presence of two or more tones the approach taken herein has been to compute the intermodulation produced by the nonlinear detector as if it is operating independently in an open-loop situation. By the computations, it has been shown that the phase detector introduces odd order spectra other than the desired components while the VCO introduces even order undesired spectra. It is reasonable therefore to assume that for unique tones, p and q, the power in the undesired spectra produced in the phase detector is not additive to the power in the undesired spectra produced by the VCO but is rather interleaved according to the exact frequency of the significant spectral lines.

To aid in interpreting the effect of the feedback loop in compensating for the component nonlinearities the quasi-linear model of Fig. 3.1 is assumed. In the diagram the intermodulation sources are assumed to be (voltage) signals additive to the forward channel of the loop at the output of the phase detector and at the input of the VCO. Since the nonlinearities involved are very small in the phase modulation application, the nominal detector and VCO sensitivities (K_d and K_{VCO}) are

sufficiently equal to the effective gains that they may be used with negligible loss of accuracy.

The effect of the respective intermodulation distortion sources may be established generally by consideration of their influence upon the system error signal which is $V_\varepsilon(t)$ in the diagram, Fig. 3.1.

1. Effect of Loop on VCO Nonlinearity: - From the model of Fig. 3.1, the voltage error $V_\varepsilon(t)$ (at the system null point is):

$$V_\varepsilon(s) = \frac{\frac{K_{VCO}\,K_d}{N\,S\,(S/\omega_1 + 1)}}{1 + \frac{K_v}{S\,(S/\omega_1 + 1)^2}} \cdot I_{VCO}(s) \qquad \text{Eq.(3.1)}$$

$$= \frac{1}{K_A} \cdot \frac{(S/\omega_1 + 1)}{\left[\frac{S^2}{\omega_n^2} + \frac{2\zeta S}{\omega_n} + 1\right]\left[\frac{S}{\omega_1} + 1\right]} \cdot I_{VCO}(s) \qquad \text{Eq.3.2)}$$

from which

$$V_\varepsilon(s) \approx \frac{1}{K_A} \cdot I_{VCO}(s) \qquad \text{Eq.3.3)}$$

for $S < \omega_1$ and K_v . This conclusion may also be visualized from the graphical representation of Fig. 3.2. The result is that VCO sensitivity may be traded for increased gain KA, and dynamic range of the driving amplifier with a significant improvement of intermodulation.

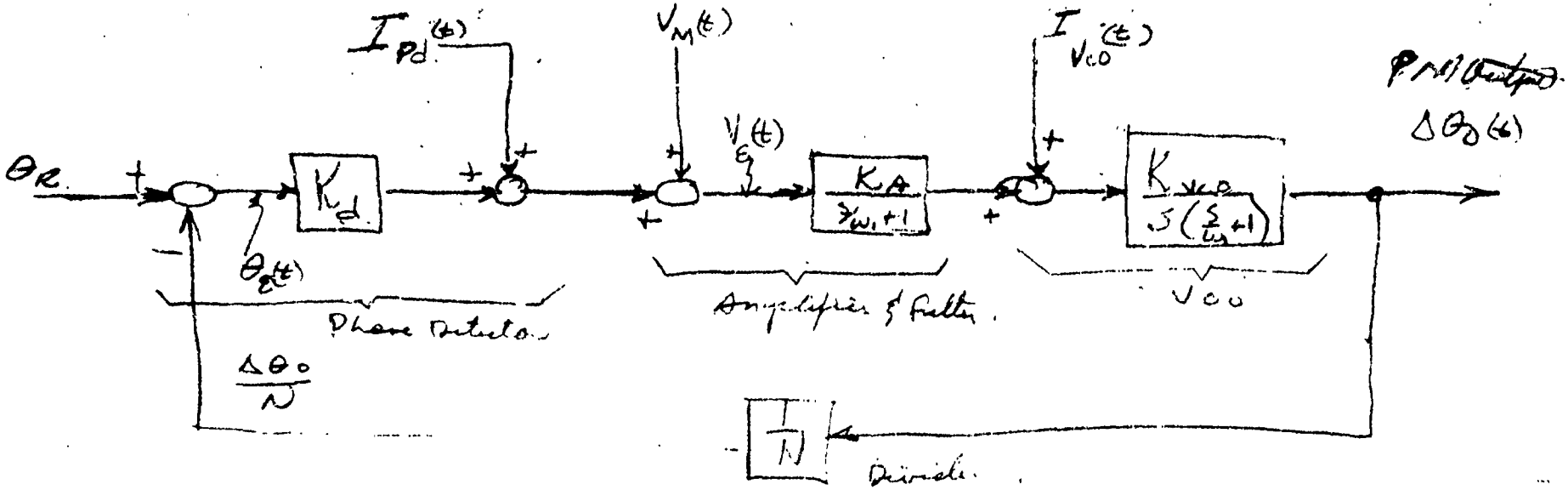

Fig. 3.1 Quasi-linear phase modulator loop with intermodulation sources.
(Diagram based on Bode-Nichols example)

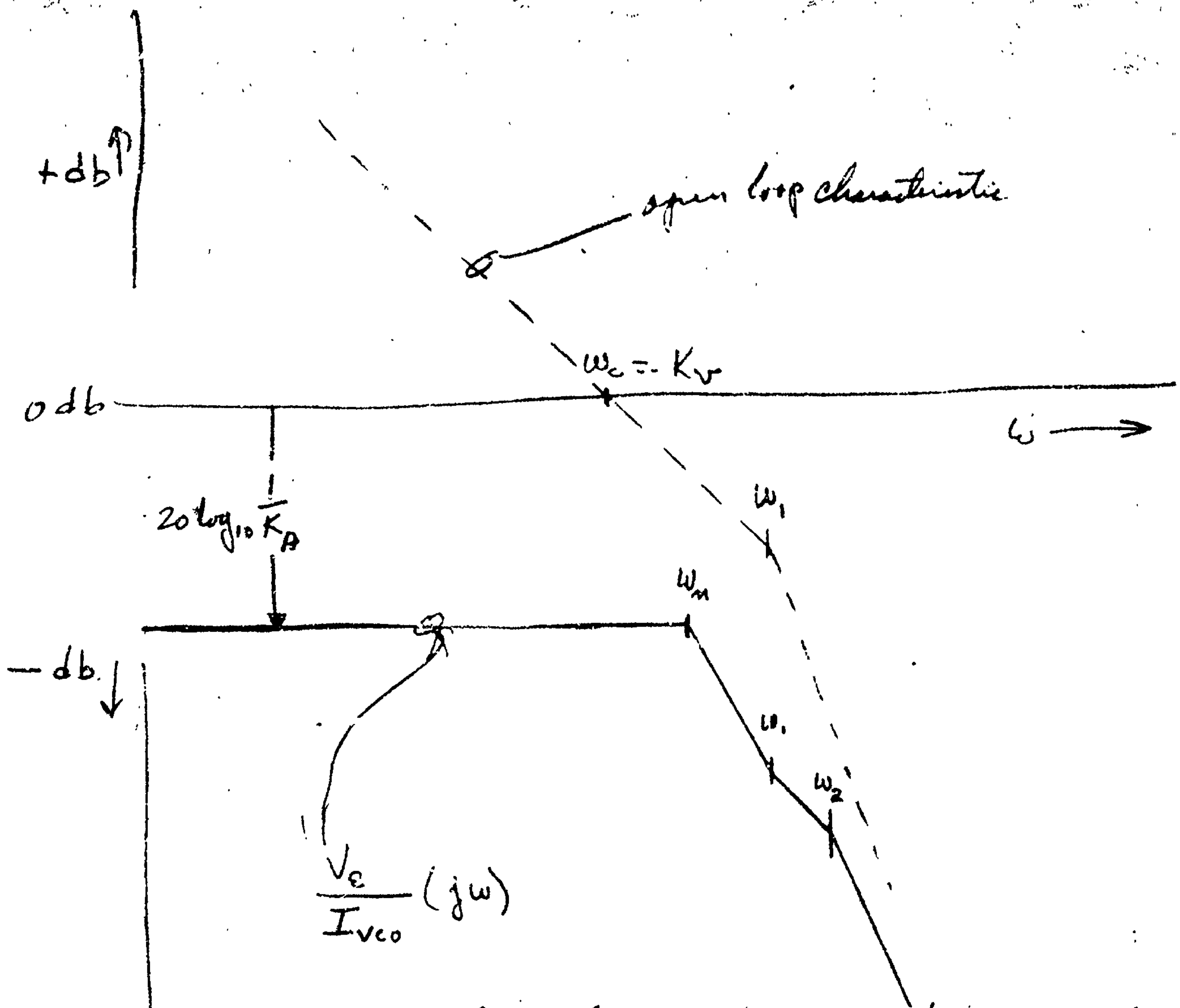

Fig 302 Error Response Characteristic to a VCO Nonlinearity.

for example, an overall gain of KA = 3.16 in the amplifier and filter combination should provide 10 db of improvement which according to Table 5b (of Section III) would permit a VCO of 1% nonlinearity with ± 4 radians phase deviation. Under such conditions the maximum even-order intermodulation is estimated to be at a level of -44 db relative to the carrier. As a tentative objective an amplifier gain of 10 is recommended, providing a liberal margin for error in the assumed VCO control characteristic and further degradation by the phase detector.

2. Effect of Loop on Phase Detector Nonlinearity:- By a similar analysis the estimate of the phase detector odd-order intermodulation source, $I_{Pd}(S)$ on the system error $V_\varepsilon(S)$ is derived:

$$V_\varepsilon(s) = \frac{1}{1 + \frac{K_v}{S\left(\frac{S}{\omega_1}+1\right)^2}} \cdot I_{Pd}(S) \qquad \text{Eq. (3.4)}$$

$$V_\varepsilon(s) = \frac{1}{K_v} \frac{S\left(\frac{S}{\omega_1}+1\right)^2}{\left[\frac{S^2}{\omega_n^2} + \frac{2\xi S}{\omega_n} + 1\right]\left[\frac{S}{\omega_2}+1\right]} \cdot I_{Pd}(S) \qquad \text{Eq. (3.5)}$$

Comparison of Eqs. (3.2) and (3.5) indicate a significant difference in the effectiveness of the loop on phase detector sources of intermodulation as compared to the VCO nonlinearity. Because of the (s) term appearing in the numerator of Eq. 3.5 the compensation is frequency sensitive, decreasing at a 6 db per octave

rate as the frequency of the components increase. The effect is illustrated graphically by the asymptotic lines of Fig. 3.3.

At very high frequencies ($\omega > \omega_c$) no improvement whatsoever will be achieved. In the region where $\omega \approx \omega_c$ no more than 3 db of compensation is possible for critically damped systems and as much as 6 db of actual degradation is possible for underdamped systems. To minimize further degradation the damping coefficient should be controlled by choosing the corner frequencies (ω_1) sufficiently large compared to ω_c .

In determining the adequacy of the system reference is directed to the unequal tone analysis summarized in Table 4 below. There p is a tone in the 0-500 KCS band and q is a tone in the 500 KCS to 1.5 MCS band, with deviations at the output of 3 and 1 radians respectively. The highest intermodulation product or harmonic of a principal tone should be about 56 db below the lowest tone (which is q in this case) after the full effect of the loop is considered.

Assuming a loop bandwidth of about 1.5 mcs little or no compensation can be expected at the top of the band (1.5 mcs). Since p may be chosen at 500 kcs then its third harmonic 3 p = 1.5 mcs would appear at the output without compensation. If at the same time q is chosen at 1.5 mcs then p + 2 q occurs at 3.5 mcs and q +2p

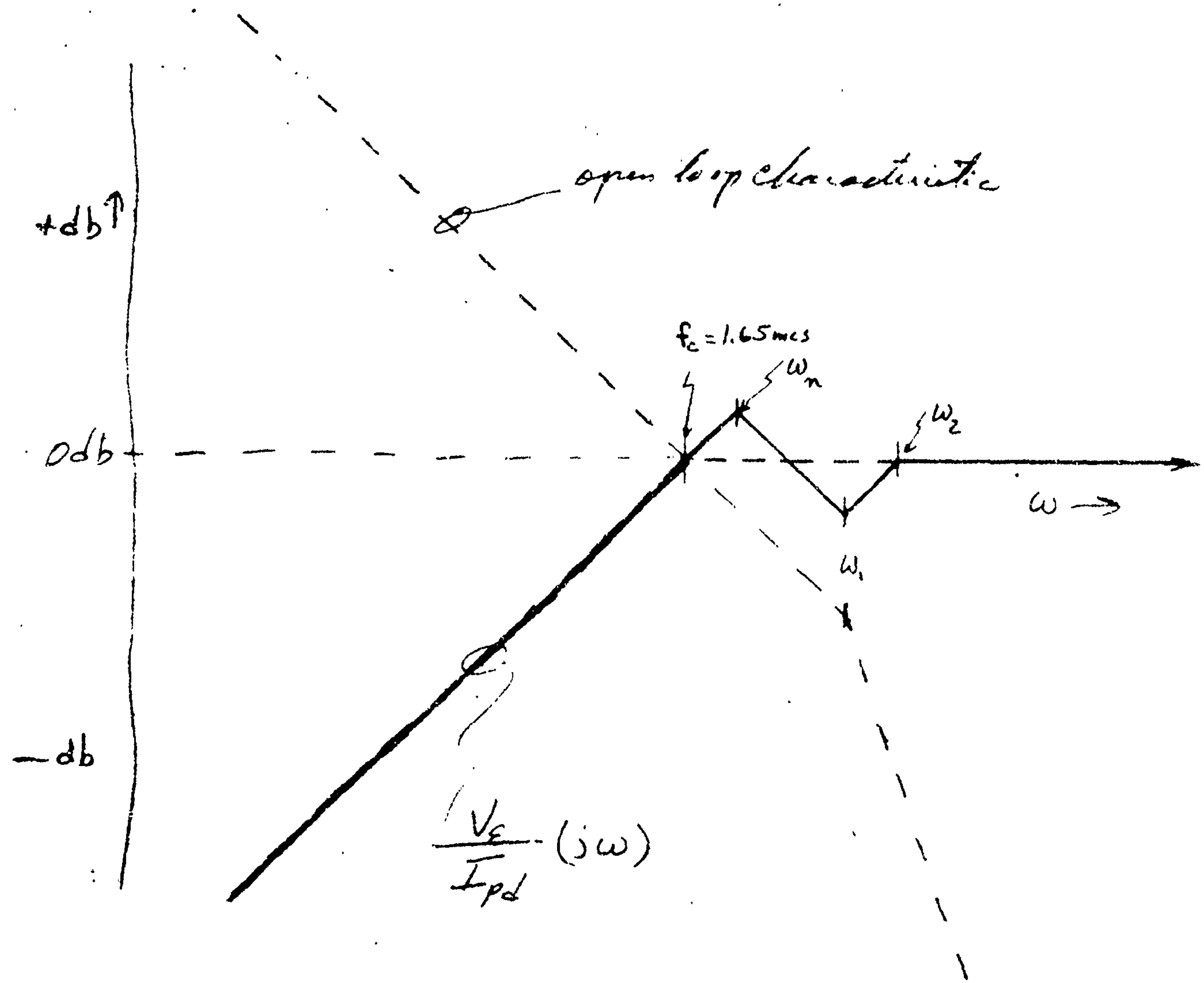

Fig 3.3. Error Response Characteristic to Phase Detector Nonlinearity
(Diagram based upon Bode-Nichols example)

occure at 4.5 mcs, neither obtaining any improvement.

In order to avoid the necessity for a broadband loop at least 2 octaves wider than the maximum modulating frequency (about 6 mcs) it appears that a detector range of $\pm \frac{\pi}{4}$ radians and a linearity of 5% or better are required if the fidelity specification is to be met at the top of the modulation band.

2. Two Tone Analysis: - For purposes of estimating preliminary performance, selection of phase detector characteristics, and specifying the linearity of components several two tone analytical studies have been performed including the following:

a. Phase detector - Sinusoidal characteristic with $\frac{\pi}{4}$ radians deviation: - Two principal questions are involved, namely: (1) Can a phase-locked phase modulator be built at the specified 50 KW level using a conventional phase detector having sinusoidal characteristics for deviations of $\frac{\pi}{4}$ radians peak, and (2) Assuming that a phase modulated signal of the specified character is developed, what will be the effect on transmitter-receiver fidelity due to the sinusoidal detector specified in the receiver in order to simulate the characteristics of the DSIF equipment?

In the analysis, the phase detector is assumed to be driven by perfect signals, one from a reference oscillator (V_R), and one (V_M) which represents an ideal two tone phase modulated signal. In this analysis the two tones are assumed to have equal levels causing a total peak deviation of $\pm$ 4 radians. The detector is of the product or sinusoidal type.

After expansion of the product, collection, and evaluation of the various Bessel coefficients, the harmonics and intermodulation frequencies related to the two tones, pand q, are calculated. These calculations are summarized in Table 1 giving the level of each frequency term relative to the principal tones, p and q.

From the calculations one must conclude: (a) in the transmitter, the use of direct feedback from the 50 mcs output to a phase detector of the sinusoidal characteristic type does not furnish a practical solution, and (b) in the receiver, assuming a perfect phase modulated wave is received, nevertheless, tremendous distortion and intermodulation will be present at the modulation output. When one considers the range of values permissible for the tones p and q, even further distortion will exist in the baseband (or demodulated) spectrum due to the foldover of those

TABLE I

Two (Equal) Tone Analysis - Sinusoidal Phase Detector at Peak Deviation of + 4 Radians

Frequency Terms		Level Relative to Tones, p and q
p	q	0 db
3p	3q	-13
5p	5q	-38.1
7p	7q	-70.5
p ± 2q	q ± 2p	+4.0
p ± 4q	q ± 4p	-16.1
p ± 6q	q ± 6p	-45.4
p ± 8q	q ± 8p	-54.5
3p ± 2q	3q ± 2p	-9.0
3p ± 4q	3q ± 4p	-29.5
3p ± 6q	3q ± 6p	-58.5
3p ± 8q	3q ± 8p	-67.5
5p ± 2q	5q ± 2p	-34.2
5p ± 4q	5q ± 4p	-54.5
5p ± 6q	5q ± 6p	-64
5p ± 8q	5q ± 8p	-72.8
7p ± 2q	7q ± 2p	-69.5

intermodulation terms which appear at negative frequencies.

Thus, in the transmitter the phase deviation of the output signal (in the feedback branch to the phase detector of the modulator) must be compressed by the action of a frequency countdown divider. With respect to the receiver, since a faithful simulation of DSIF equipment is emphatically specified, one must recognize that $\pm$ 4 radian phase deviation over a $\pm$ $\pi/2$ degree sinusoidal phase detector must necessarily result in large intermodulation products.

b. Phase Detector - Sine Characteristic with $\pm$ 1 Radian Deviation: - For reasons set forth below a feedback frequency divider of ratio of 4 to 1 is selected which would ideally require the phase detector of the transmitter to operate at a peak deviation of one radian. For this condition an analysis was made for the application of two equal tones, p and q, to the product detector. The significant harmonic and intermodulation frequencies arising as a result of the detector nonlinearity are summarized in Table 2.

Compared to the results obtained for 4 radian peak deviation, the tabulation indicates a large reduction in the level of harmonic and intermodulation frequencies. The convergence is very rapid, yet the third harmonic and third order intermodulation levels are higher than the fidelity specification would permit. It will be shown in a later worksheet that, for distortion created at the phase detector, the feedback loop will tend to compensate, rejecting the undesired frequency components by the

TABLE 2

Two (Equal) Tone Analysis - Sinusoidal Phase Detector at Peak Deviation of ± 1 Radian

Frequency Terms		Level Relative to Tones, p and q
p	q	0 db
3p	3q	-39.5
p ± 2q	q ± 2p	-28.8
p ± 4q	q ± 4p	-72.5
3p ± 2q	3q ± 2p	-68.2
3p ± 4q	3q ± 4p	—

inverse of the equivalent open-loop gain. The compensation is, therefore, frequency sensitive and reduces to unity in the region near the loop bandwidth. To provide sufficient loop gain to reduce the third order terms to less than 46 db below the modulated carrier would require excessive loop bandwidth. Hence, the product detector operating at signal phase deviations of 1 radian cannot be recommended because of the nonlinearity of the sine characteristics.

c. Phase Detector - Linearized $\pm \pi$ Radians with $\pm$ 1 Radian Deviation: - In order to meet the fidelity requirements, a phase detector of the linearized or saw-tooth type is recommended. Eliminating auxiliary frequency dividers and considering the basic detector above the maximum nominal linearity is assumed to be limited to phase error angles of less than $\pm \pi$ radians, The linearity of the detector saw-tooth characteristic is expressed by a power series giving the output, v, as a function of the phase error, θ_e :

$$v = a_1 \theta_e + a_2 \theta_e^3 + a_3 \theta_e^5 - \cdots - a_n \theta_e^{2n-1} \qquad \text{Eq. (3.6)}$$

If the characteristic is an odd function, i.e., $v(\theta_e) = -v(-\theta_e)$ then all even powers of θ_e will be absent and only odd order harmonic and intermodulation products will be present in the detector output. In the computations, the first two terms of the power series are assumed significant. Again a two tone analysis is performed to estimate the degree of nonlinearity permissible. To avoid confusion

with feedback loop performance, the detector is examined in an open loop condition with a perfect reference signal and an ideal two tone phase modulated signal as inputs.

General equations are written for computing the frequency spectrum in terms of the deviation $\Delta\theta$, and tones p and q. The degrees of nonlinearity is expressed by the factor M which is the percentage of droop of the output voltage from linearity as measured at the limits of the sawtooth range ($\pm \pi$). With equal tones and a peak phase deviation of $\pm$ 1 radian the third order harmonic and intermodulation products are as given in Table 3 for 1, 5, and 10% nonlinearities.

Table 3. Two (Equal) Tone Analysis — Linearized Ohare Detector at peak Deviations of ± 1 radian.

Linearity (Droop)	Detector Range ± π: M FACTOR	Signal Levels — clip: p	q	3p	3q	p ± 2q	q ± 2p	Detector Range ± π/2: M FACTOR	Signal Levels — db: p	q	3p	3q	p ± 2q	q ± 2p
1%	100	0	0	-83.9	-83.9	-74.4	-74.4	25	0	0	-71.9	-71.9	-62.4	-62.4
5%	~~20~~	0	0	-70	-70	-60.5	-60.5	5	0	0	-57.8	-57.8	-48.3	-48.3
10%	10	0	0	-61	-64	-54.5	-54.5	2.5	0	0	-49.1	-49.1	-39.6	-39.6

65-335 Appd

9/

d. Phase Detector - Linearized $\pm \pi/2$ radians with $\pm$ 1 radian deviation: - The analysis discussed in (c) immediately was extended for a simplified detector of line-based sawtooth range over $\pm \pi/2$ radians phase error. As might be expected for the same peak deviation of $\pm$ 1 radian and with comparable nonlinearities the intermodulation is correspondingly worse. The computations for equal tones is summarized also in Table 3.

e. Phase Detector - Linearized with deviation by two unequal tones:- For simultaneous narrow-and-wideband modulation, levels for a two-tone test are to be weighted according to the diagram in Figure 1.2 where the tone "p" is confined to frequencies from dc to 500 kcs and "q" is confined to frequencies between 500 kcs and 1.5 MCS. In order to finalize objectives for the phase detector required in the modulator, consideration of the unequal levels is required. Two open-loop computations of the de-detector performance have therefore been repeated for unequal tones "p" and "q" in a 3 to 1 ratio. The results are summarized in Table 4 with relative levels given in DB with respect to both tones "p" and "q". For purposes of specifying phase detector linearity the harmonics and inter-modulation terms should be compared to the lowest level tone -"q", in this case. For example, using a sawtooth detector of range $\pm \pi$ radians, a 5% linearity in the open loop situation produces third harmonics of the the tone "p" which are only 53.4 db below the desired tone "q". Should "p" be selected near 500 Kc then 3 p will occur near 1.5 mcs. This is the top of the band where the loop gain approaches unity (more or less) depending upon the equivalent gain and exact loop bandwidth.

Table 4. Unequal Two Tone Analysis, Linearized Channel Detector at ± 1 radian peak

Linearity (Droop)	M Factor	Detector Range ± π radians. Signal levels — db						M Factor	Detector Range ± π radians. Signal levels — db					
		P	Q	3P	3Q	P±2Q	Q±2P		P	Q	3P	3Q	P±2Q	Q±2P
1%	100	0	-9.5	-76.9	-105.5	-76.9	-96.4	25	0	-9.5	-64.8	-73.4	-64.8	-64.3
		+9.5	0	-67.4	-96	-67.4	-76.9		+9.5	0	-55.3	-83.9	-55.3	-64.8
5%	20	0	-9.5	-62.9	-91.5	-62.9	-72.4	5	0	-9.5	-50.6	-79.5	-50.6	-60.1
		+9.5	0	-53.4	-82	-53.4	-62.9		+9.5	0	-41.1	-69.8	-41.1	-50.6
10%	10	0	-9.5	-56.9	-85.5	-56.9	-65.4	2.5	0	-9.5	-44.3	-78.1	-44.5	-54.0
		+9.5	0	-47.4	-76	-47.4	-56.9		+9.6	0	-35.1	-63.6	-35.0	-44.5

Because the power series for the detector may also require a small contribution from the 3rd term ($a_3 \theta_e^5$), and because further distortion will enter due to the imperfections of the VCO control, it is recommended that as a design objective a linearized phase detector of range $\pm \pi$ radians and a linearity of 5% or better shall be required.

f. VCO linearity requirement: -In addition to the phase detector nonlinearity the designer of a wideband phase-locked phase modulator must also allow for inherent nonlinearity of the VCO. Here again the two tone analysis is a useful tool for preliminary estimation of the linearity required.

Arguments Supporting a Two-Tone Analysis of VCO Linearity: - It is general knowledge that a VCO has an output frequency about its normal value which is a function of the applied signal. Ideally the frequency shift should be directly proportional, i.e., a linear function of applied voltage. But the nature of the control circuit is inherently nonlinear. The VCO may be biased into a limited operating range, $\pm \Delta f$, wherein the frequency shift, Δf_{error} is an even order function of the control voltage. Graphically, we have,

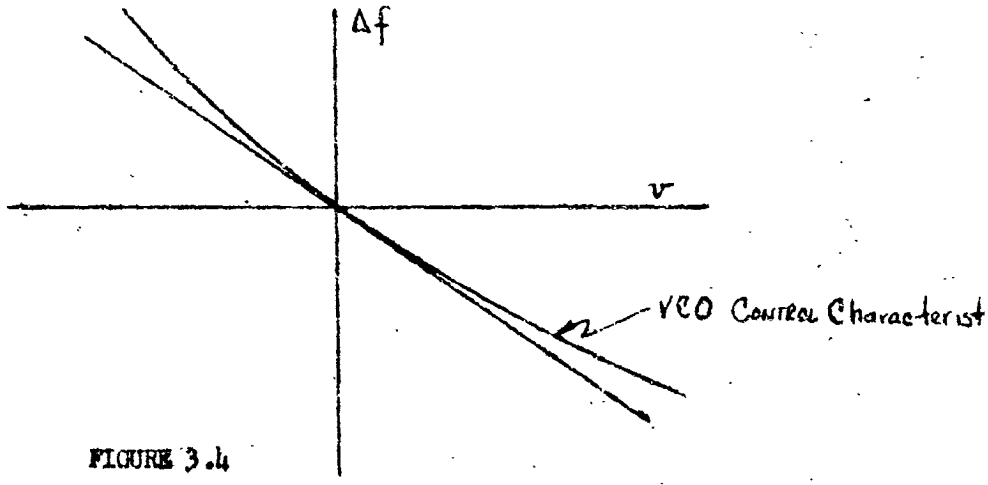

FIGURE 3.4

The characteristic shown in (Figure 3.4) applies to the VCO as a component element standing alone It is the transfer function for the component in an open loop configuration

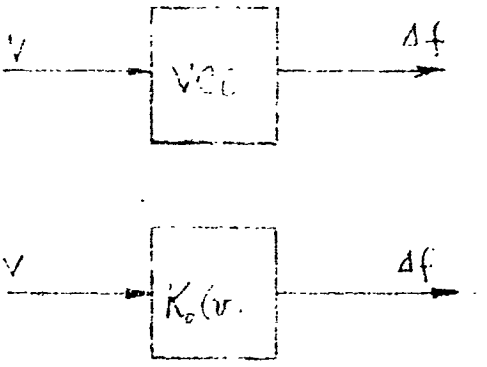

FIGURE 3.5

As shown in the diagram of Figure 3.5. K_o is the sensitivity which is nonlinear with the applied voltage, v. As the applied voltage becomes a dynamic function of time it is obvious that the VCO is inherently a frequency modulation device.

When used as a component in a phase-locked loop the output signal of the VCO is forced to comply with phase variations of a reference signal or other driving function. For example, in the phase modulator application under investigation, the output is phase modulated according to variations of a low pass spectrum, V. In simplest form, we have.

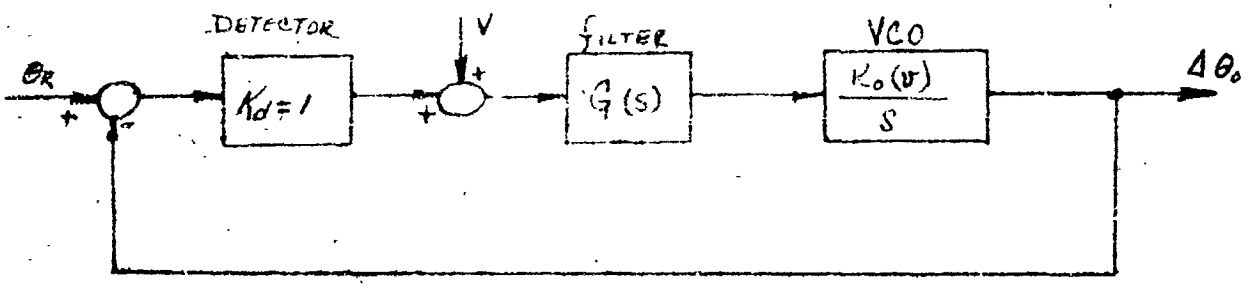

FIGURE 3.6

In this simple case: $\frac{\Delta\theta_2}{\Delta\theta_1}(s) = \frac{1}{1 + \frac{5}{s(s)\,K_0(v)}}$

or $\Delta\theta = V$ if $\omega \gg \omega_{max}$ Equation (3.7)

One will observe that open loop investigation of two tone intermodulation for a phase modulation output are not logically performed.

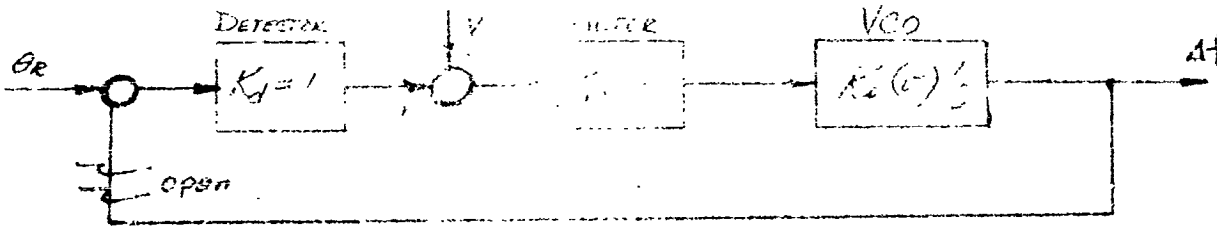

FIGURE 3.7

In the open loop Figure 3.7 the VCO is free running and with respect to the modulating signal. The conditions in a low pass frequency band are the same as in Figures 3.4 and 3.5. We cannot obtain the desired function $\frac{\Delta\theta_2}{\Delta\theta_1}(s)$, since the VCO is basically a frequency modulator.

To aid in the study of the effects of VCO nonlinearity in a phase-locked phase modulator it is helpful to return to the closed loop, but with a modified block diagram, Figure 3.8.

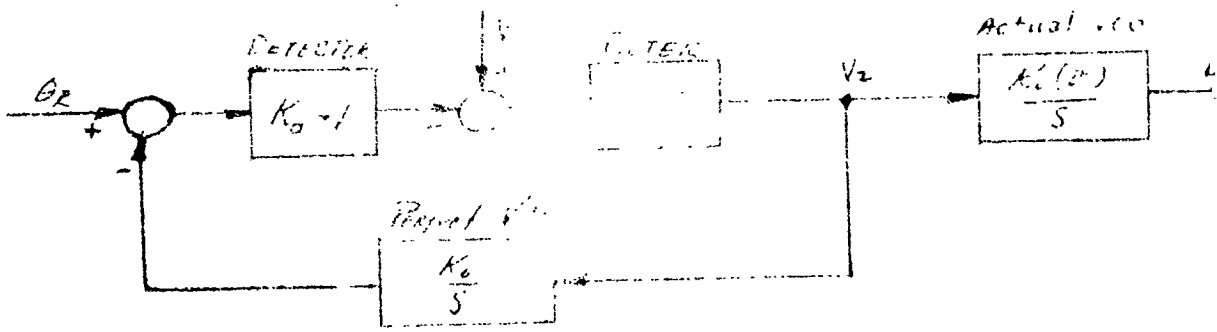

FIGURE 3.8

In this diagram the loop is closed by a perfect (or model) VCO placed in the feedback path while the nonlinear VCO is in an output branch outside the loop. The model VCO has the same nominal sensitivity as the physical unit under study. The block diagram is equivalent to the basic model of Figure 3.6 as can be shown by writing the transfer function.

$$\frac{\Delta\theta}{V} = \frac{K_o(v)}{K_o} \cdot \frac{1}{1 + \frac{S}{G(s)K_o}} \qquad \text{Equation (3.8)}$$

Since $K_o/K_o(v) \simeq 1$, we may say,

$$\frac{\Delta\theta}{V} \simeq \frac{1}{1 + \frac{S}{G(s)K_o}}$$ as before. We now have a perfect phase-locked loop cascaded with a drift-free but nonlinear VCO. The transfer function of the perfect phase locked loop may be substituted in its place.

$$\frac{V_2}{V}(s) = \frac{1}{K_o} \cdot \frac{S}{1 + \frac{S}{G(s)K_o}} \qquad \text{Equation (3.9)}$$

or $\frac{V_2}{V}(s) = \frac{S}{K_o}$, if $G(j\omega)K_o \gg j\omega_{max}$.

The model loop in Figure 3.8 is therefore a simple perfect differentiator of sensitivity $\frac{1}{K_o}$. The block diagram may be further reduced to

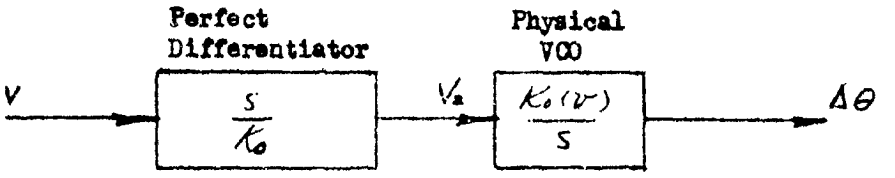

FIGURE 3.9

From this the combined circuit is simply

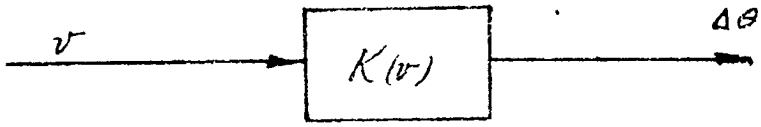

FIGURE 3.10

where $K(v) = \frac{K_o(v)}{K_o}$. This analysis confirms the obvious conclusion that if PM is desired when using a frequency modulator then a 6 db per octave pre-emphasis is required.

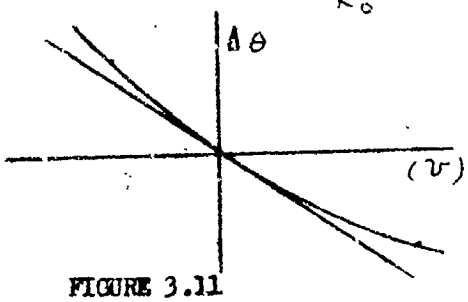

FIGURE 3.11

The conclusion to be drawn from this argument is that for the combination of a physical VCO, having nonlinearity, together with an otherwise perfect phase-locked loop, a two-tone analysis of intermodulation is valid. Furthermore the analysis is valid where the combined characteristic is taken as in Figure 3.11. The nonlinearity of the output phase vs. control voltage of the combined circuit is due to the nonlinearity of the VCO above. With appropriate scale factors the Δf ordinate of Figure 3.4 may be changed to $\Delta\theta$ in Figure 3.11 reflecting the desired operation.

The two-tone analysis approach is the same as used above for the linearized phase detector. However, the error (deviation from linearity) of the control characteristic as illustrated in Figure 3.11 above, is assumed to be an even function of the modulating voltage, v, when viewed about the nominal operation point. As a consequence it may be expected that even order harmonics and intermodulation products will predominate. This is shown to be true by the computations below, where it is assumed that a square law characteristic exists. For convenience in making the computations, one may estimate the open loop phase modulation due to two equal tones assuming a translation in frequency from the 50 mcs carrier to dc.

A rigorous analysis for two-tone phase modulation of a nonlinear deviable oscillator at its carrier frequency proved to be too laborious for hand computation. Analysis of ideal two-tone modulations can be found in the literature, but this writer has been unable to discover successful rigorous analysis of the nonlinear case. The results of our

simplified [illegible] are listed in table 5(a) showing the relative [illegible] of the principal sidebands, second order harmonics and intermodulations.

The tabulation is not completely satisfactory because the fidelity specifications for two-tone signals refer the requirement to carrier levels rather than to the modulation frequencies themselves. A convenient technique suggested by Dr. Edsel Worrall leads to a practical estimation. This method proceeds as follows:

$$Q = -K\left(v - \frac{v^2}{MV}\right) \qquad \text{Equation (3.10)}$$

but $v = V(\sin pt + \sin qt)$ for two equal tones

$$(v)^2 = V^2 \sin^2 pt + \text{[illegible]} + 2\sin pt \sin qt$$

$$\frac{(v)^2}{MV} = \frac{V}{M}\left[\frac{1}{2} - \frac{1}{2}\cos 2pt + \text{[illegible]} \cos (p-q)\,t\right.$$

$$\left. - \cos (p+q)\,t + \frac{1}{2} - \frac{1}{2}\cos 2qt\right]$$

thus max intermodulation term relative to either tone is

$$\frac{IM}{Tone} = 20 \log_{10} \frac{1}{M} \qquad \text{Equation (3.11)}$$

Table 5(a) VCO Linearity - Two Tone Analysis, ± 4 radians peak deviation

Deviation from Linearity	M factor	Signal Levels of Spectral Components -DB					
		p	q	2p	2q	p-q	p+q
0.2%	500	0	0	-60	-60	-54	-54
0.5%	200	0	0	-52	-52	-46	-46
1.0%	100	0	0	-46	-46	-40	-40
2.0%	50	0	0	-40	-40	-34	-34

(b) Estimates with Respect to Carrier Frequency,

Deviation from Linearity	M factor	Signal Levels of Spectral Components -DB						
		ω_o	$\omega_o \pm p$	$\omega_o \pm q$	$\omega_o \pm 2p$	$\omega_o \pm 2q$	$\omega_o \pm (p-q)$	$\omega_o \pm (p+q)$
0.2%	500	0	+6	+6	-54	-54	-48	-48
0.5%	200	0	+6	+6	-46	-46	-40	-40
1.0%	100	0	+6	+6	-40	-40	-34	-34
2.0%	50	0	+6	+6	-34	-34	-28	-28

The oscillator output is

$$Y(t) = A \cos \left[\omega_0 t + \Delta\theta f(t) \right] \qquad (3.12)$$

By substitution and grouping we have

$$Y(t) = A \cos \left\{ \underbrace{\left[\omega_0 t - K v(t) \right]}_{\text{desired}} + \underbrace{\frac{K v^2(t)}{MV}}_{\text{Nonlinear}} \right\} \qquad (3.13)$$

Expanding trigonometrically

$$Y(t) = A \left\{ \cos(\omega_0 t - K v(t)) \cos \frac{K v^2(t)}{MV} - \sin(\omega_0 t - K v(t)) \sin \frac{K v^2(t)}{MV} \right\}$$

if $M \gg K\bar{V}$, then

$$\frac{Y}{A}(t) = C_0 \cdot (\omega_0 t - K v(t)) - \frac{K v^2(t)}{MV} \sin(\omega_0 t - K v(t))$$

$$\frac{Y}{A}(t) = \cos(\omega_0 t - K v(t)) - \frac{K\bar{V}}{M} \left[\sin^2 pt + 2 \sin pt \sin qt + \sin^2 qt \right] \sin(\omega_0 t - K v(t)) \qquad (3.14)$$

from which

$$\frac{IM}{CARRIER} = 20 \log_{10} \frac{K\bar{V}}{M} = -20 \log_{10} \frac{1}{M} + 20 \log_{10} K\bar{V} \qquad (3.15)$$

But $|\Delta\theta| = K\bar{V} = 2$, for two-equal tones and a peak deviation of $\pm$ 4 radians, $\therefore$ $\frac{IM}{CARRIER}$ is 6 DB lower (poorer) than $\frac{IM}{TONE}$, therefore, the carrier level must be 6 DB below the principal tones.

On the basis of this estimate it is now possible to reconstruct the tabulation of frequency components as has been done in (b) of table 5.

Examination of Table 5(b) implies that a loop design having all the gain in the VCO (therefore having no loop compensation) VCO linearity of the order of onehalf percent should be adequate. Further discussion of the probable compensatory effect of the phase-locked feedback loop on nonlinearity at the VCO is presented below to show that VCO linearity may be relaxed.

C. Effect of Transportation Lag:

The transportation lag (or time delay) due to non-minimum phase relationships within the feedback loop is the ultimate limiting factor on the permissible stable bandwidth of the feedback loop. The effect is expressed by the unit vectors (e^{-sT}) as shown in Figure 3.12 which represents the preliminary design using the Bode-Nichol's procedure. Delays occur in both the feedforward and feedback channels of the loop.

For the phase modulator it is estimated that the time delays are approximately $T_1 = 3.5 \times 10^{-9}$ sec,
$T_2 = 15 \times 10^{-9}$ sec.

Taken around the loop $e^{-s(T_1+T_2)} = e^{-j\omega(T_1+T_2)} = 1 \angle \phi_T$

$$\phi_T = \omega\left(T_1 + \frac{T_2}{2}\right)$$

$=$

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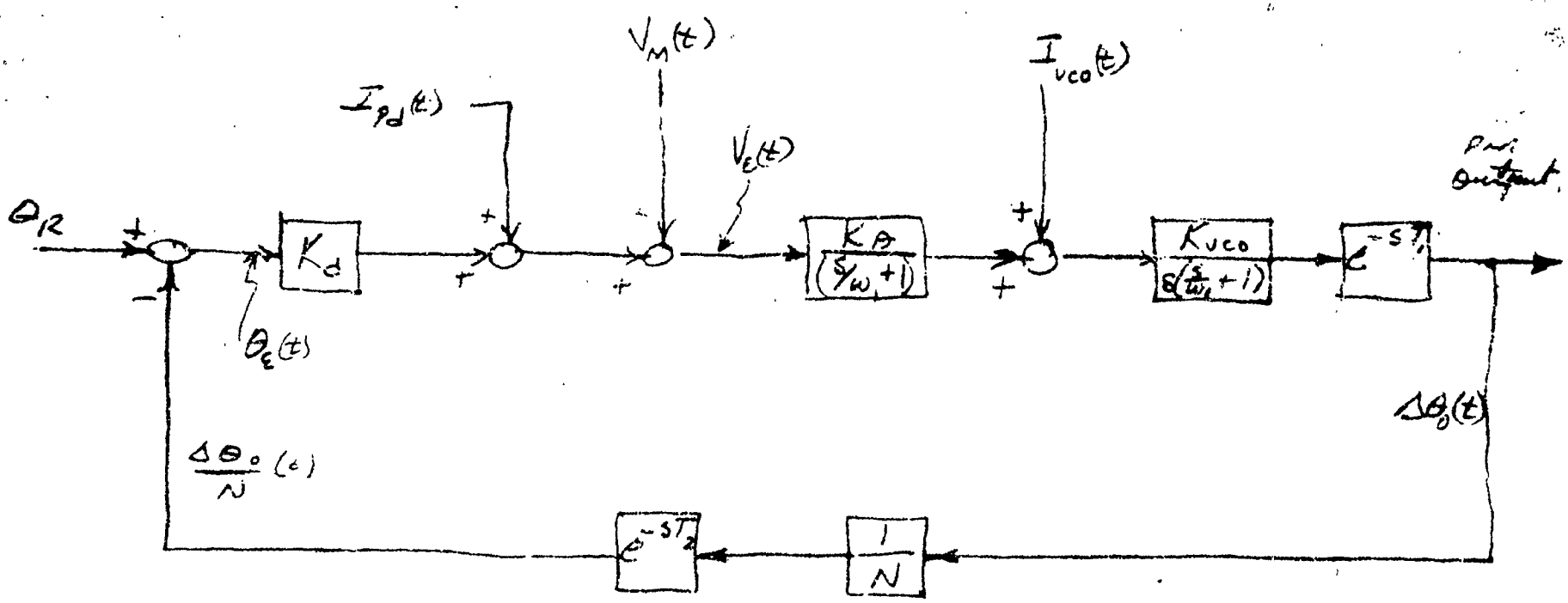

Fig 3.12 Quasi linear Model with Transportation Lags.
(Diagram based on Bode-Nichols Example).

In the neighborhood of unity gain the effect of transportation lag on loop stability as expressed in terms of phase margin is calculable by

$$\phi_m = +\frac{\pi}{2} - 2 \arctan \frac{\omega_c}{\omega_1} - \left(\phi_T = \omega_c (T_1 + T_2)\right] \qquad \text{Eq (3.17)}$$

At ω_c, $\phi_T = 2\pi \times 1.63 \times 10^6 \times 18.5 \times 10^{-9}$ radians

$= 11$ degrees

The desired phase margin is therefore reduced by 11 degrees which would slightly alter the relative stability of the loop. However if the loop bandwidth W_c were increased by an octave the transport lag would become serious, requiring an upward adjustment of the filter and VCO corner frequencies at W_1 for comparable stability margins.

On the Nichol's chart of Figure 2.2 the dashed curve was drawn to account for the additional phase accumulation due to the lag terms. It may be seen that transport lag causes a tangency to a higher constant amplitude contour, hence the peaking of the frequency response at the top of the modulation band increases. Figure 2.2 suggests that excessive peaking of the frequency response in the presence of transportation lag may be avoided by a simple reduction of open loop gain (with a corresponding decrease of loop bandwidth). Should such gain

adjustment be required the possibility exists that some compensation external to the loop may be necessary in order to achieve the desired overall bandwidth.

From Equation (3.16) it is noted that phase due to transport lag is directly proportional to frequency, therefore this factor does not contribute to variations in group delay.

D. Incidental AM:

It has been determined that the weak frequency deviation of the VCO is produced by the narrow-band signal and amounts to ± 2.0 mcs. At the carrier frequency of 50 mcs the operation of the oscillator will be 12.5. To achieve the linearity specified it is recommended that the oscillator operate Class A with [illegible]. With this concept incidental AM is minimized consistent with the transmitter-receiver fidelity requirement.

E. Signal Assymetry and DC Bias:

Assymmetry and DC bias will result in the assumption by the phase detector of an operating point off center and will cause the linearities predicted herein will not be valid. We therefore recommend that steps be taken to eliminate any DC components introduced by the modulating signal generators in [illegible].

IV.

A. Implementation of Circuits

The Locked oscillator Phase Modulator block diagram is repeated in figure 4.1

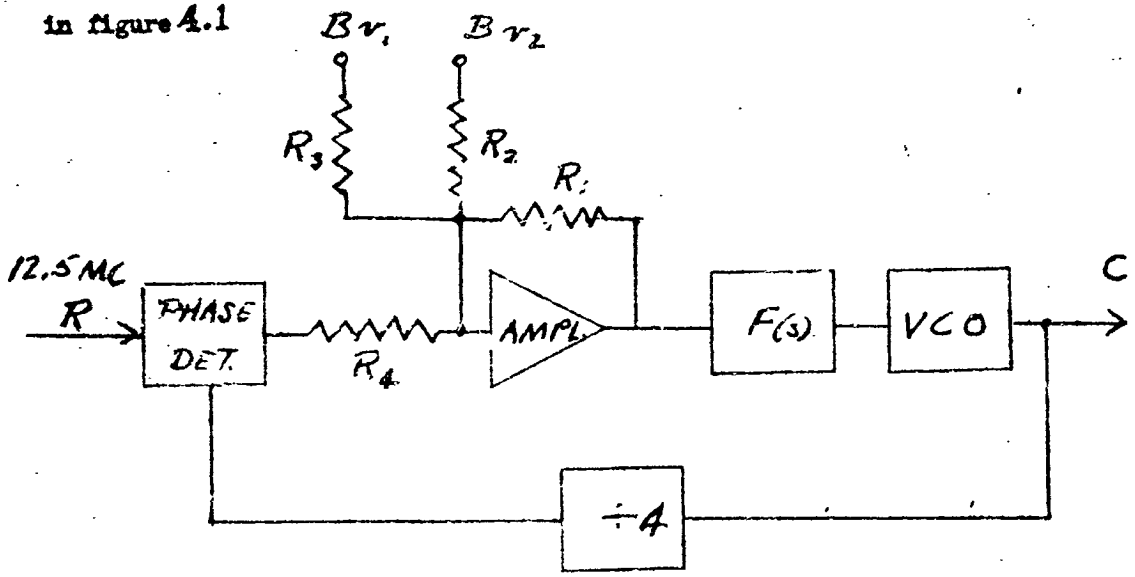

FIGURE 4.1 Locked Oscillator Phase Modulator

The circuit parameters are listed as follows:

Loop Amplifier

The loop amplifier provides a convenient summing point to inject the modulating signals Bv1 and Bv2 at relative levels indicated in Figure 4.2.

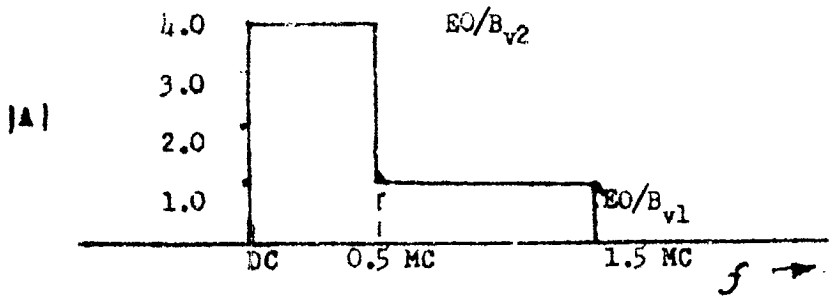

FIGURE 4.2 Modulating Signal Levels

Ideally, the amplifier amplitude response shall not contribute to the allowed ± 0.1 db droop at 0.5 MC and ± 0.5 db droop at 1.5 MC. Aside

from providing a means of summing the modulating signals, the loop amplifier must provide a forward loop gain of 10.

Two amplifiers were considered. The Philbrick SP-456 (the chopper stabilized version of the Philbrick P-45) and an existing Westinghouse design. Both amplifiers have essentially the same characteristics (the Westinghouse amplifier is not chopper stabilized); namely, a closed loop 3 db bandwidth of 15 MC at unity gain.

As the closed loop gain is increased, the 3 db bandwidth decreases at a rate of 6 db per octave. The voltage transfer of $\frac{EO}{Bv_2}$ shall be minus unity and the transfer $\frac{EO}{Bv_1}$ minus one fourth. The minimum 3 db bandwidth in both cases is 15 MC. The amplitude droop at 0.5 and 1.5 MC is 0.000434 db and 0.0536 db respectively as expressed by equation 4.1

$$\frac{K}{K_o} = \sqrt{\frac{1}{1 + (f/f_{3DB})^2}} \qquad (4.1)$$

The amplifier droop contribution to Bv_1 and Bv_2 is neglected.

The Philbrick amplifier 3 db bandwidth at a closed loop gain of 10 is 1.5 MC. The Westinghouse amplifier closed loop unity gain 3 db bandwidth can be extended to 50 MC with modification. The 3 db bandwidth at a closed loop gain of 10 is 5MC. The designer may choose to use the loop amplifier pole as a portion of the overall loop

transfer function or cancel the pole with a lead-lag network at the amplifier loop forward gain input. The latter choice is more attractive. Refer to figure 4.3

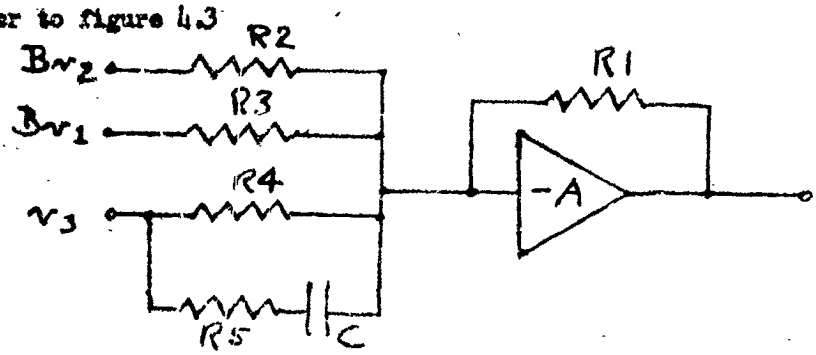

FIGURE 4.3 Loop Amplifier Compensation

The transfers are listed as follows:

$$\frac{E_o}{B_{V_1}} = \frac{R1}{R3} \qquad (4.2)$$

$$\frac{E_o}{B_{V_2}} = \frac{R1}{R2} \qquad (4.3)$$

$$\frac{E_o}{V_3} = \frac{R1}{R4}\left[\frac{1 + S(R4 + R5)C}{1 + S\,R5\,C}\right] = \frac{R1}{R4} f_1(S) \qquad (4.4)$$

$$f_1(S) = \frac{1 + S/W1}{1 + S/W2} \qquad W1 = \frac{1}{(R4+R5)C}\,, \quad W2 = \frac{1}{R5C} \qquad (4.5)$$

Let $W_1 = 2\pi \times 1.5 \times 10^{+6}$ rad/sec (4.6)

Let $W_2 = 2\pi \times 15 \times 10^{+6}$ rad/sec (4.7)

Figure 4.4 indicates the compensated amplifier response. The Philbrick SP-456 operational amplifier is suitable for this application.

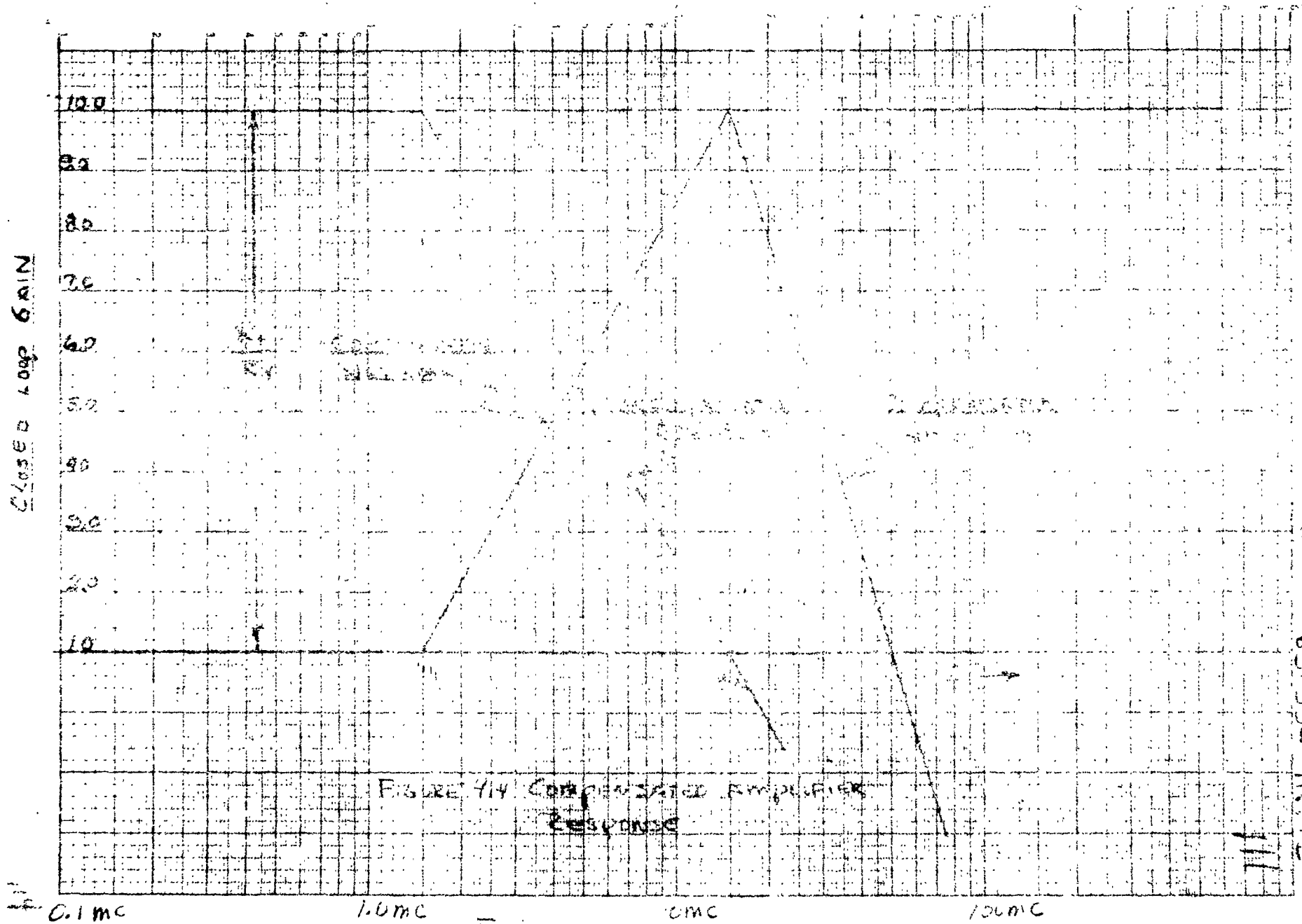

FIGURE 7/4 COMPENSATED AMPLIFIER RESPONSE

2. Voltage Controlled Oscillator

The VCO contribution to the loop transfer function is $\frac{K_{VCO}}{S(\frac{S}{W_1}+1)}$. The corner W_1 is related to the VCO frequency and Q as indicated by equation (4.9).

$$B.W. = \frac{f_o}{Q} \qquad (4.8)$$

$$W_1 = \frac{B.W.}{2} \qquad (4.9)$$

There are two choices available for the application of W_1 to the overall loop transfer function. The corner W_1 can be made one of the principal contributors to the loop transfer function or W_1 can be made intentionally large such that its influence is ignored. A computer investigation of the closed loop peaking (3 pole Butterworth) contributed by W_1 as a function of its relationship to the closed loop cut off frequency, W_c, indicates the following: $W_1 \geq 5\ W_c$ 0.74 db peaking, $W_1 \geq 10\ W_c$ 0.34 db peaking.

The case $W_1 \geq 10\ W_c$ was investigated. Let W_c be $2.5 \times 2\pi \times .10^{+6}$ rad/sec (a typical cut off frequency as outlined earlier in this report), W_1 becomes $25 \times 2\pi \times 10^{+6}$ rad/sec.

If the VCO center frequency is selected as 50 MC the oscillator Q is one. If the VCO center frequency is selected as 450 MC an oscillator Q of 10 will yield W_1 as $22.5 \times 2\pi \times 10^{+6}$ rad/sec. The latter case is considered. The specified 50 MC phase deviated carrier is derived by down converting the 450 MC with 400 MC in a balanced strip line mixer. The diagram of this system is indicated in figure 4.5. The 12.5 MC and 400 MC are derived from the 1 MC Transmitter Frequency Standard.

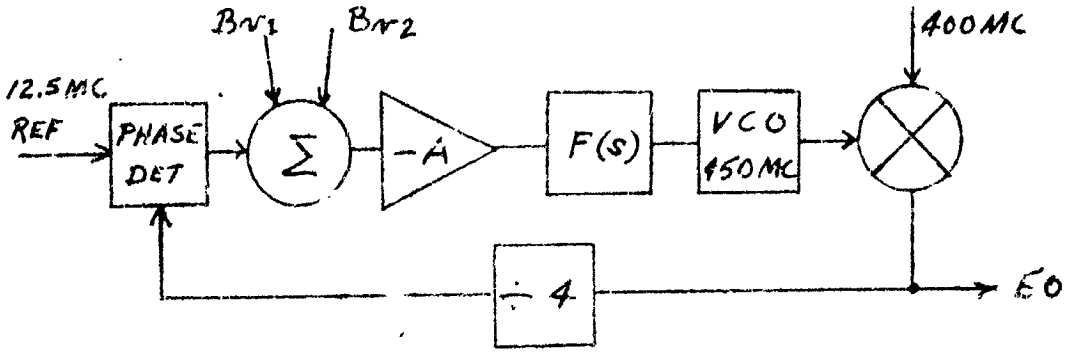

FIGURE 4.5 Simplified Diagram of Phase Modulator, 450 MC VCO

This system has the following advantages:

a) a realizable oscillator Q b) Small percentage deviation of the VCO and greater linearity. The disadvantages include: a) Increased VCO frequency drift in the unlocked mode b) Mixer Spurious contributions.

A refinement of this system is shown in figure 4.6.

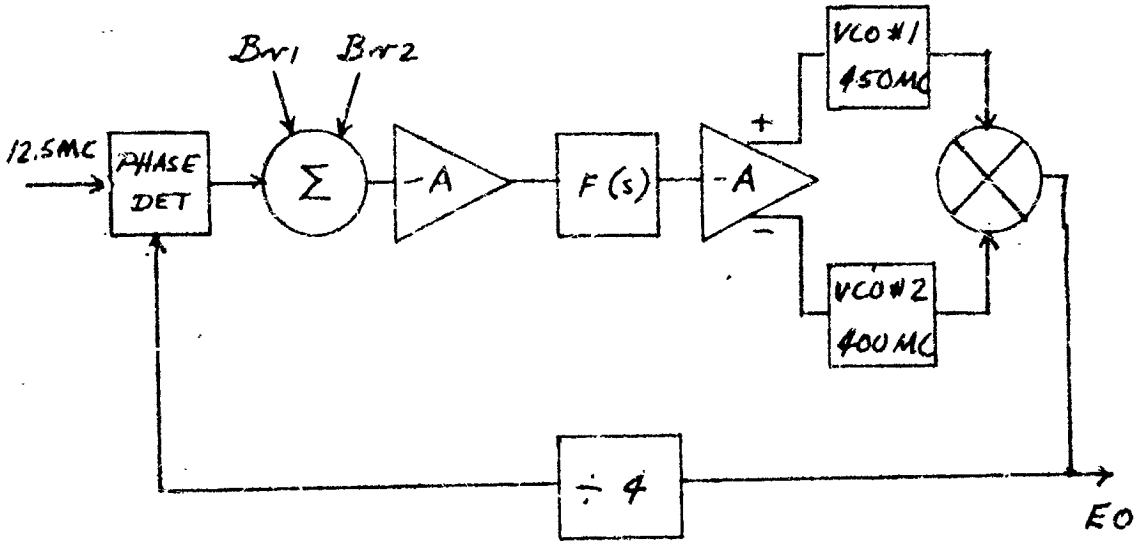

Figure 4.6 Simplified Diagram Phase Modulator, Push-Pull Oscillators

The two voltage controlled oscillators are driven push-pull. If the transfer of $\frac{f_o}{e_{IN}}$ of the two oscillators track, the non linearities of $\frac{f_o}{e_{IN}}$ cancel. Further, the total deviation of each oscillator is

one half the total. The down conversion has no influence on the deviation.

The oscillator design is straight forward. A basic design exists that is not entirely suitable for this project but at least provides a background.

Briefly, the oscillator design is based on the following considerations. The transistor model is considered a two port device as shown in figure 4.7.

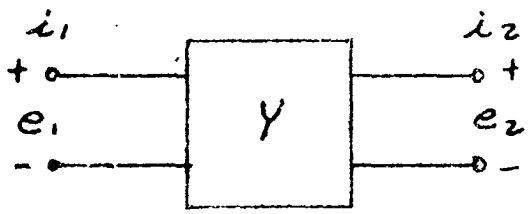

Figure 4.7 2 Port Network

$$i_1 = y_{11} e_1 + y_{12} e_2 \qquad (4.10)$$

$$i_2 = y_{21} e_1 + y_{22} e_2 \qquad (4.11)$$

A transistor connected in common base and its equivalent two port model is indicated in figure 4.8.

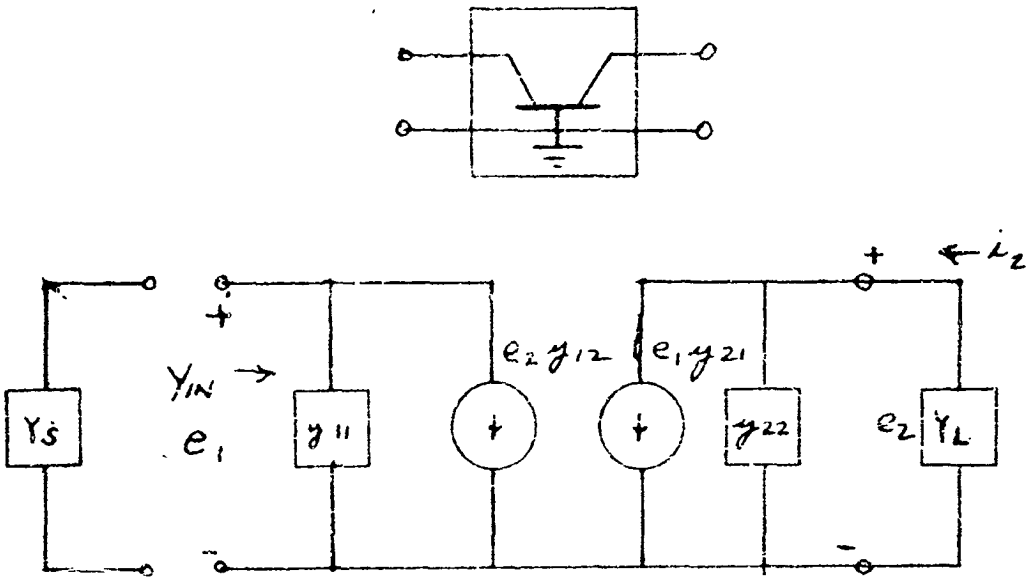

Figure 4.8 Transistor Common Base Two Port Model

The input admittance Y_{IN} is:

$$Y_{IN} = y_{11} - \frac{y_{12} y_{21}}{y_{22} + Y_L} = G_{IN} + jB_{IN} \qquad (4.12)$$

It is obvious that if $\frac{y_{12} y_{21}}{y_{22} + Y_L} \geq y_{11}$ such that G_{IN} (real part of Y_{IN}) is negative the device is potentially unstable. Bahrs(1) has shown that $G_{IN} = \frac{1}{g_{11}} \left[g_{11} g_{22} - \frac{M}{2}(1 + \cos\theta) \right]$ where $M \angle \theta = y_{12} y_{21}$. Consider the case where the two port operates between a load and generator such that $G_A = g_{11} + G_S$ and $G_B = g_{22} + G_L$. The condition for potential instability is $G_A G_B \leq M/2\ (1 + \cos\theta)$. In a practical manner this means that if the source and load conductance, G_S and G_L are large, one condition for instability is fulfilled. Further, if the sum of the angles of $(y_{11} + Y_W)$, equation 3, exceed the angle of $y_{12} y_{21}$ the

(1) "Amplifiers Employing Potentially Unstable Units", By George Bahrs, Doctors Thesis, Stanford University, 1956.

second condition exists for instability; namely, the proper phase relationship between output and input. Therefore, if the transistor source and load have large conductance and proper susceptances the device is unstable. The connection in figure 4.9 fulfills these requirements.

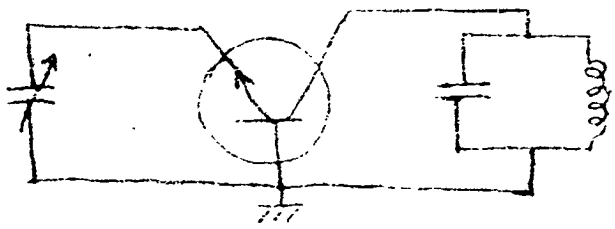

Figure 4.9 Basic Oscillator Circuit

A transistor oscillator was designed based on these consideration for a previous task. The collector tuned circuit was a quarter wave shorted line enclosed in a cavity. The line length was made variable by an adjustable shorting bar. The oscillator is tunable over the band 300-550 MC. The oscillator was made electronically tunable (VCO), aside from the mechanical tuning, by connecting a varicap across the quarter wave line. The outputs are taken from the cavity by adjustable capacitive probes. The output power is a function of emitter current. A coaxial detector was arranged to measure the oscillator power and an AGC system used to maintain the power constant against frequency variations. Figure 4.10 is the circuit diagram. Figure 4.11 and 4.12 indicate typical characteristics of f_o/E_{in} and $P_o/I_{emitter}$. The f_o/E_{in} transfer shown in figure 4.11 indicates the characteristic at the high frequency end of the band (550 MC); however, the same general shape of the transfer curve is applicable at 400 and 450 MC.

CIRCUIT DIAGRAM

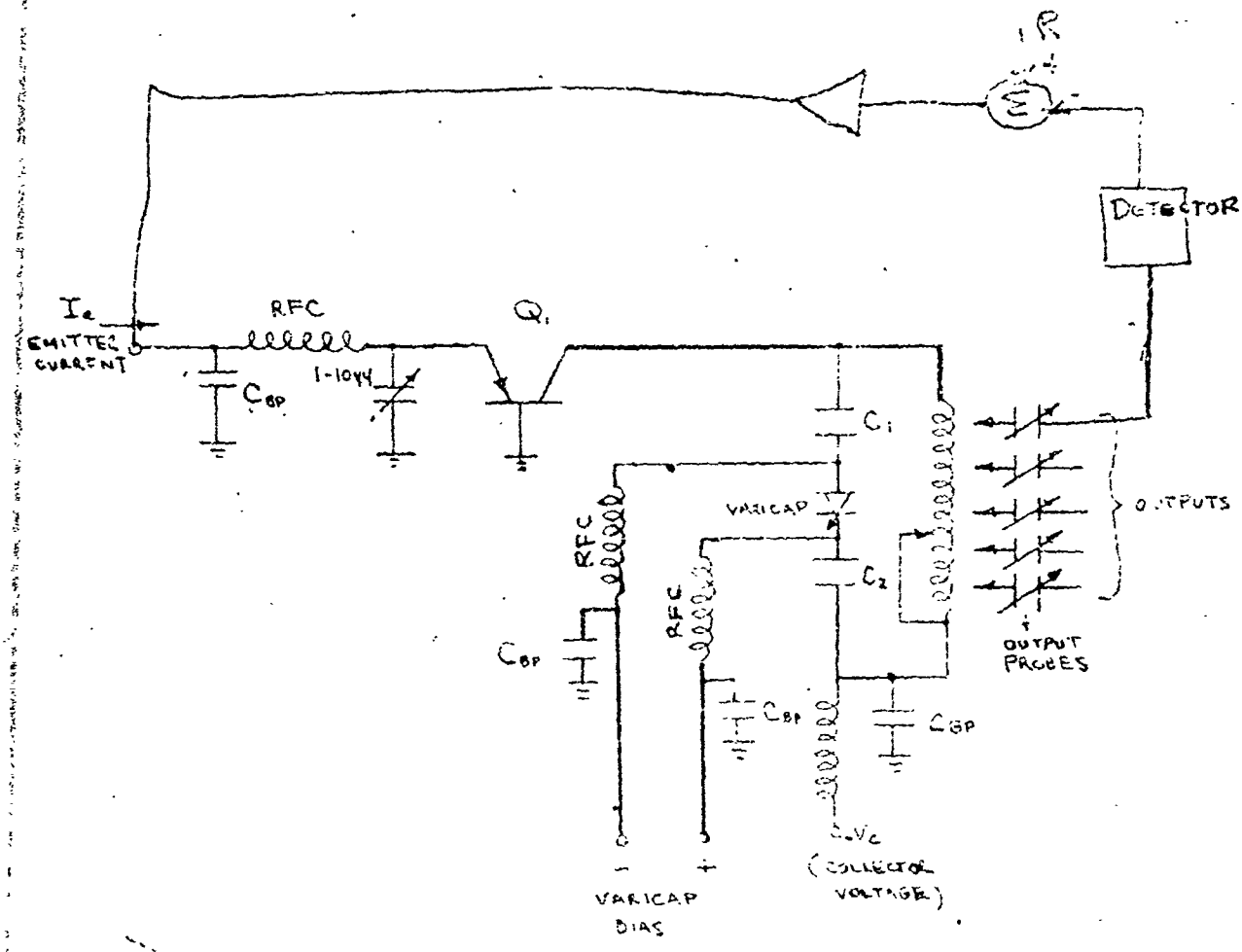

FIGURE 4.10

TUNABLE VCO (500-550mc) and AGC System

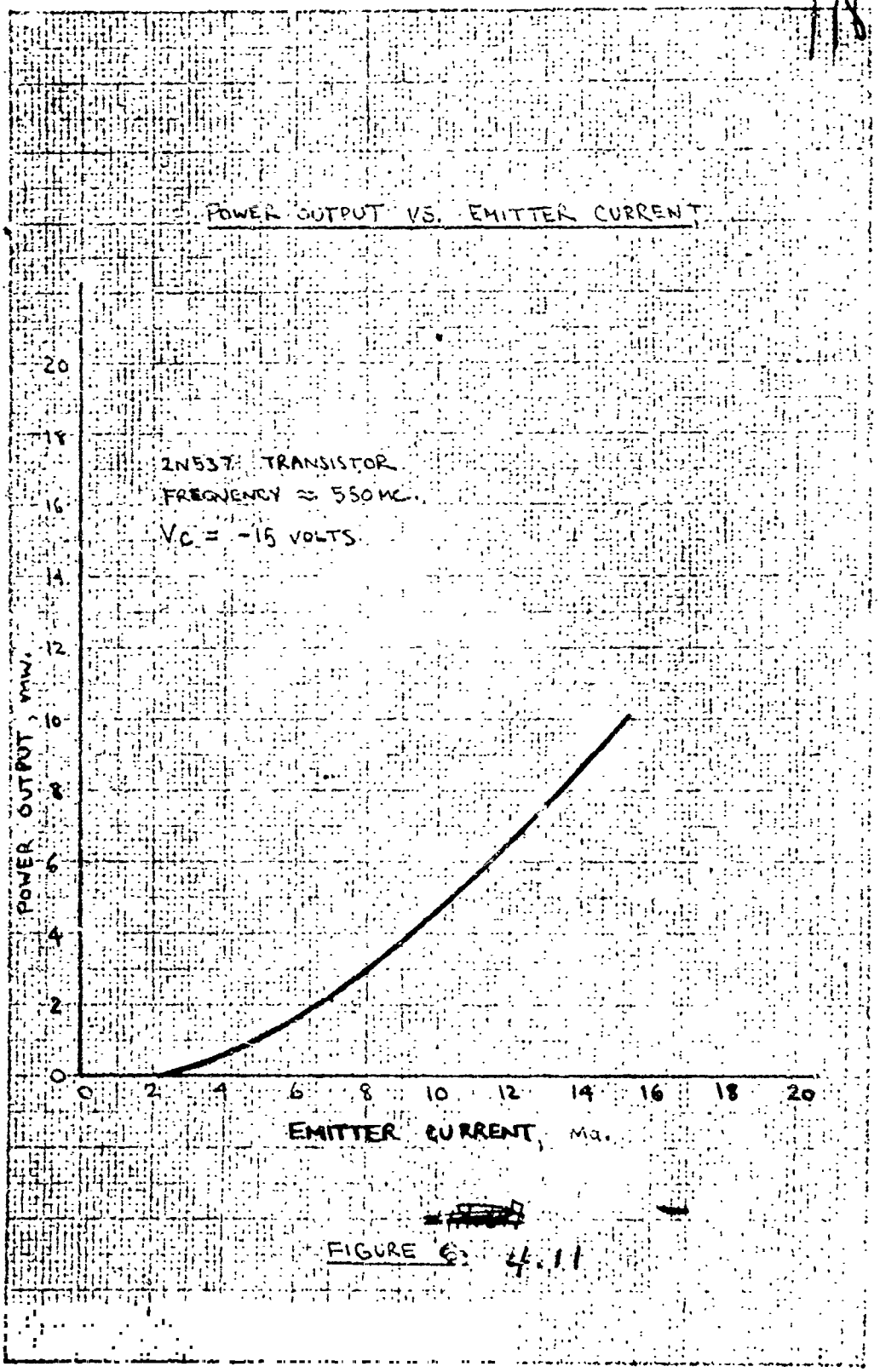

FIGURE 4.11

SIGNATURE_____ DATE_____ CURVE NO._____

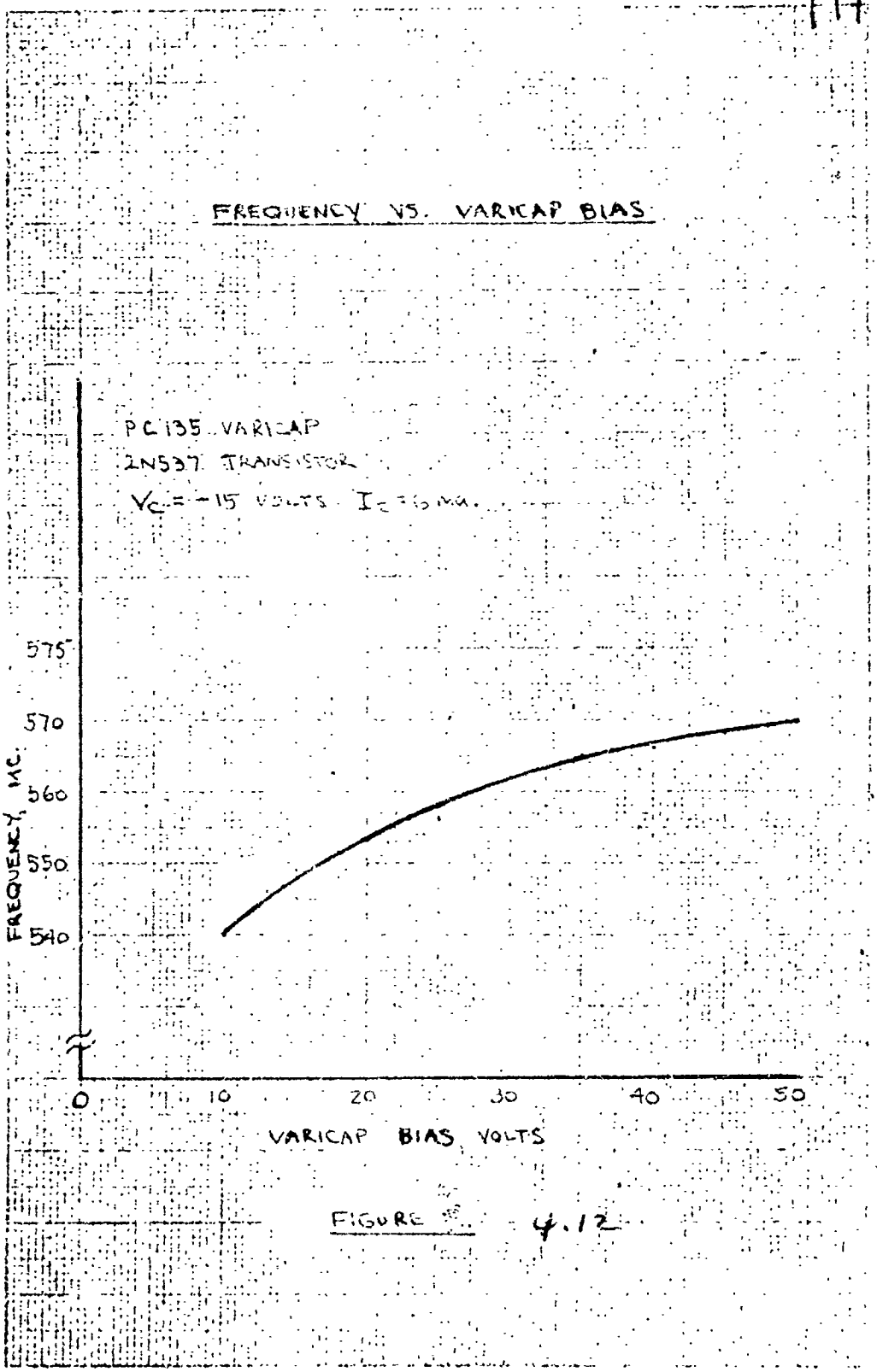
FREQUENCY VS. VARICAP BIAS
PC135 VARICAP
2N537 TRANSISTOR
V_C = -15 VOLTS I_E = 6 MA.
575
570
560
550
540
FREQUENCY, MC.
0
10
20
30
40
50
VARICAP BIAS VOLTS

FIGURE 4.12

3. Balanced Mixer

The push-pull VCO investigation includes the following mixer considerations. A stripline balanced mixer design exists from a previous task. The unit is not suitable for this project but the basic approach is applicable.

The mixer configuration consists of a microwave phasing structure and two matched diodes. The phasing structure is a folded stripline hybrid ring. A simplified diagram is shown in figure 4.13.

The stripline dimensions are cut for branch circuit impedances of 50 Ω and ring impedance of 70.7 Ω.

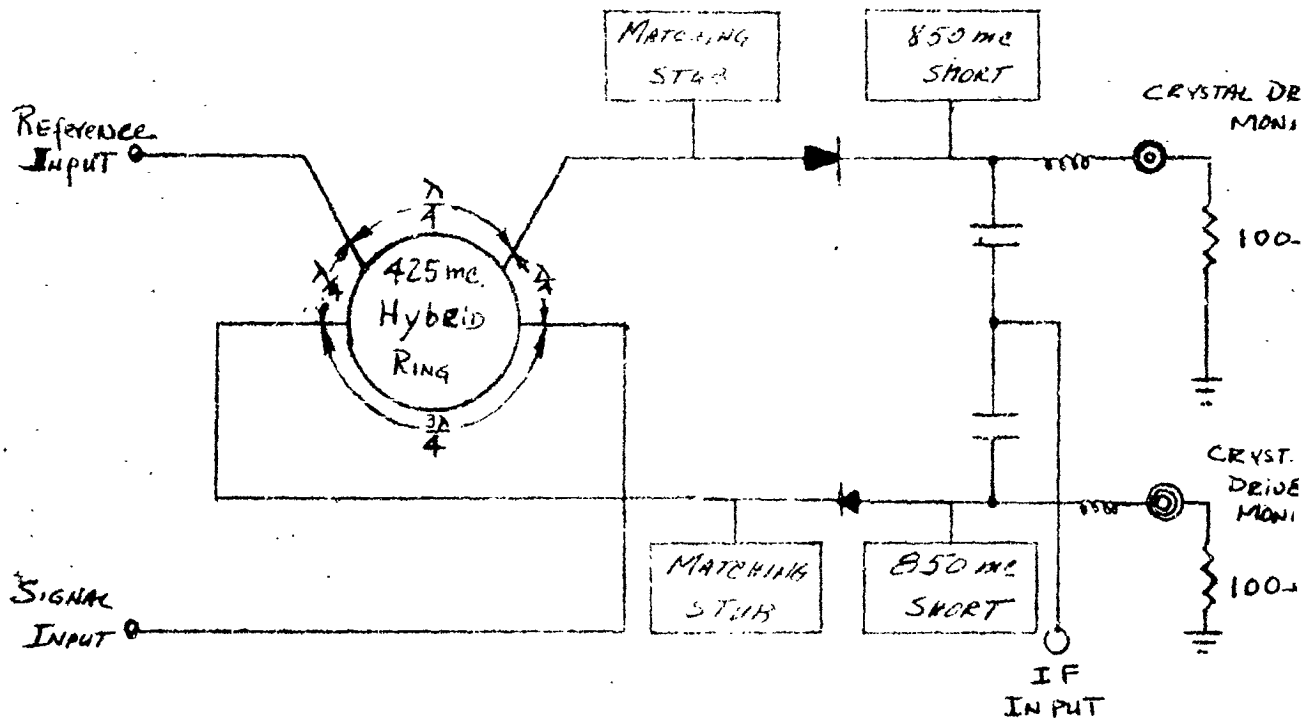

Figure 4.13 Simplified Stripline Balanced Mixer

The design proved [illegible] and matched [illegible] between signal source [illegible] between diode characteristics and [illegible] signal sources.

The local oscillator and signal level through the IF output is 40 db below the signal. [illegible] signal levels are 0 dbm and -20 dbm. The corner [illegible]

The output power [illegible] to drive the feedback divider. In addition, the minimum signal [illegible] is typically -8 dbm. The divider input requires [illegible] Hot carrier diodes are available (1N 3682) that will provide [illegible] of both the local oscillator and signal [illegible] approximately 200 mw. The VCO power [illegible] to the level. The alternative is to add an amplifier between [illegible] divider. However, an amplifier's delay contribution [illegible]

e. Conclusions

The conclusions drawn from this [illegible] system are summarized as follows: The 450 MC and 200 MC pulsed [illegible] mixer offer the advantage listed. However, this system is complicated. The mixer spurious will introduce time jitter in the [illegible] divider. The additional component add loop delay. Therefore, the recommended system consists of a single 50 MC VCO with the oscillator Q designed such that the VCO corner, ω_1 ($\frac{K_{VCO}}{S(\frac{S}{\omega_1}+1)}$) is an integral part of the loop transfer function.

The [illegible] is taken from the [illegible] oscillator circuit rather than on the [illegible] because it has an extremely linear, [illegible] is required to level the output [illegible] of a similar unit designed [illegible] Hall. The oscillator design equations are included in [illegible] available. The circuit diagram is shown in [illegible] The [illegible] K_{sub}, of this unit shown is approximately $\frac{\text{[illegible]}}{\text{volt}}$ at 70 kc.

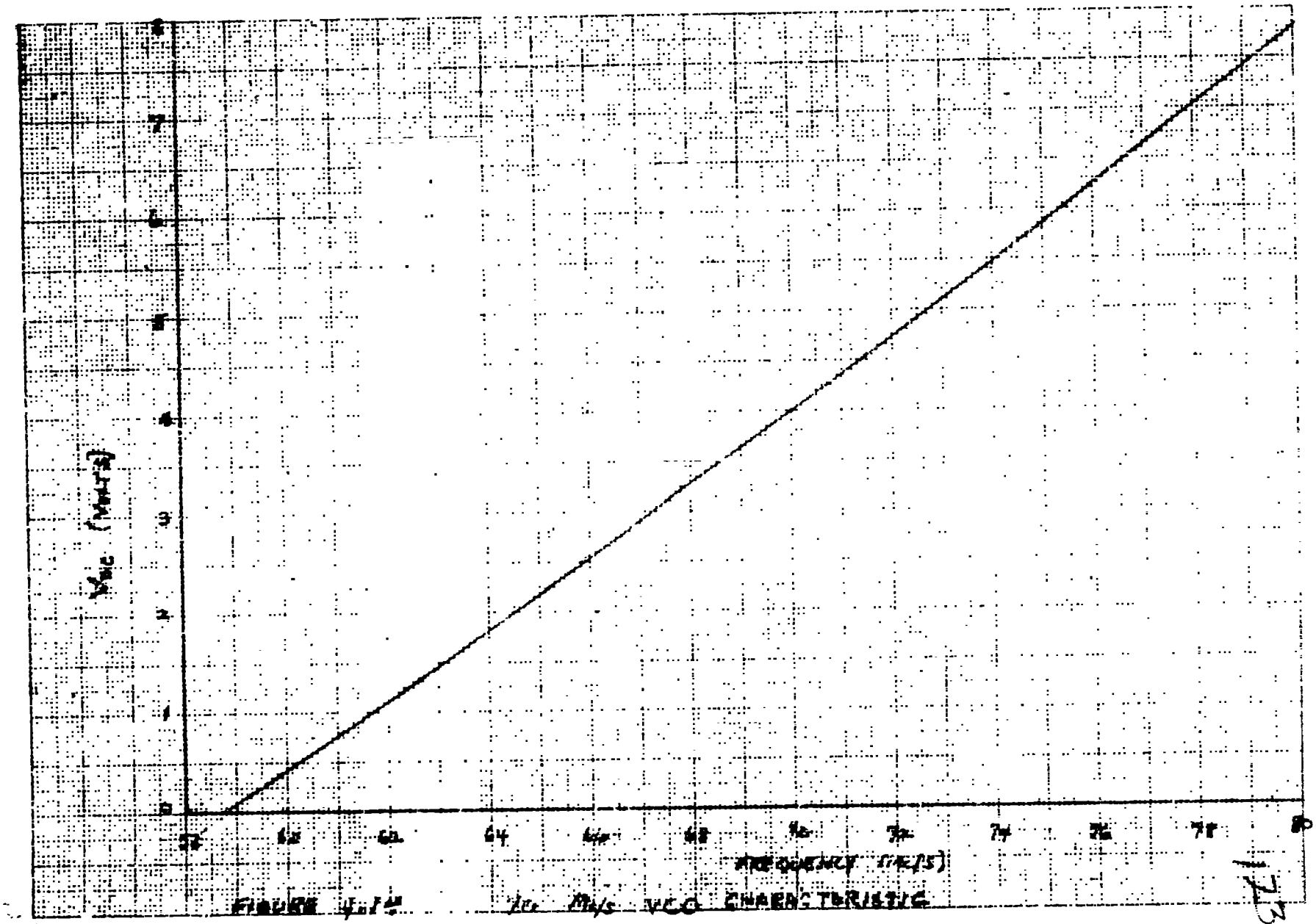

FIGURE 4.14 Xtr. Mfg's VCO CHARACTERISTIC

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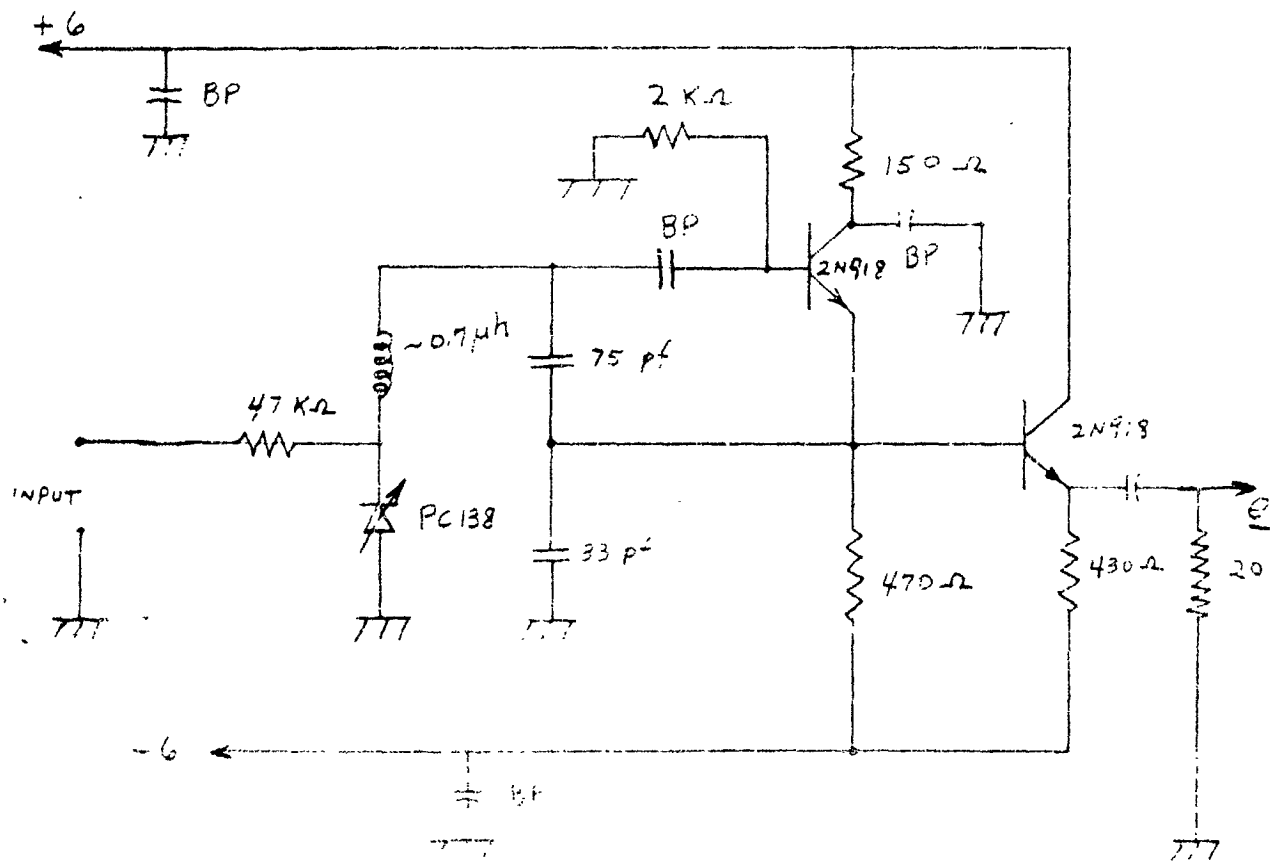

FIGURE 4.15 70 Mc/s VCO CIRCUIT DIAGRAM

4. Feedback Divider

The feedback divider converts the 50 mc at the VCO output to 12.5 mc at the phase detector input. The 50 mc phase deviation is compressed from ± 4 radians to ± 1 radian. The divider parameters of interest include: 1) Maximum toggle speed 2) Delay. Binary division at a 50 mc toggle frequency was beyond the state of the art until recently. In the past year Westinghouse has developed basic thin film digital packages with maximum toggle frequency in the 50-60 mc region. Recent development of transistors with gain bandwidth products of 2.5 kmc extends the forecast toggle speed to 100 mc. Presently the higher frequency transistors have not been incorporated in the designs. The test data of the present thin film units includes:

1.0 Flip Flop

1.1 Per Stage Propogation Delay -- 4 nanoseconds
(average of the set and reset output delays)

1.2 Maximum Toggle Speed ------- 60 mc

2.0 Stroke Gate (NAND)

2.1 Propagation Delay -------- 3.5 nanoseconds

2.2 Maximum Gating Frequency ----- 60 , mc

3.0 Squaring circuit

3.1 Propagation Delay -------- 5 nanoseconds

3.2 Maximum Squaring Frequency ----- 60 mc

The feedback divider will consist of a squarer and two flip flops arranged as a parallel-clocked binary counter as indicated in figure 4.16.

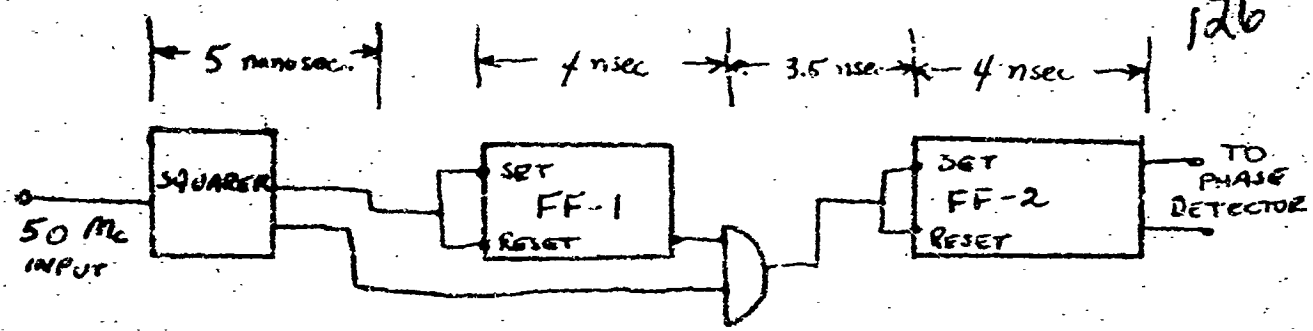

Figure- 4.16 Simplified Diagram of Feedback Divider.

The time delay as indicated is 16.5 nanoseconds but the parallel-clocking effectively eliminates the delay of FF-1, thus reducing the delay to 12.5 nanoseconds. The forecast time delay of the system with the latest transistors is 10 nanoseconds serial. 7 microseconds parallel-clocked.

5. Phase Detector

The phase detector output must be a voltage which is a linear function of the phase of the feedback divider output relative to the reference clock.

The maximum phase deviation at the 50 mc carrier frequency is ± 4 radians. The equivalent maximum phase deviation at the divider output is ± 1 radian. The phase detector linearity requirements, referenced to earlier in this report, apply to the region of ± 1 radian.

Three phase detector configurations have been considered 1) Flip Flop Sawtooth Phase Comparator 2) Modulo Two Adder Correlator 3) Early-Late Gate Correlator.

a. Flip Flop Sawtooth Phase Comparator

This Phase Detector is simply a Reset-Set (R-S) Flip Flop followed by a low pass filter. The low pass filter in this case is the loop filter. A simplified diagram of this system and the timing diagram is shown in figure 4.17.

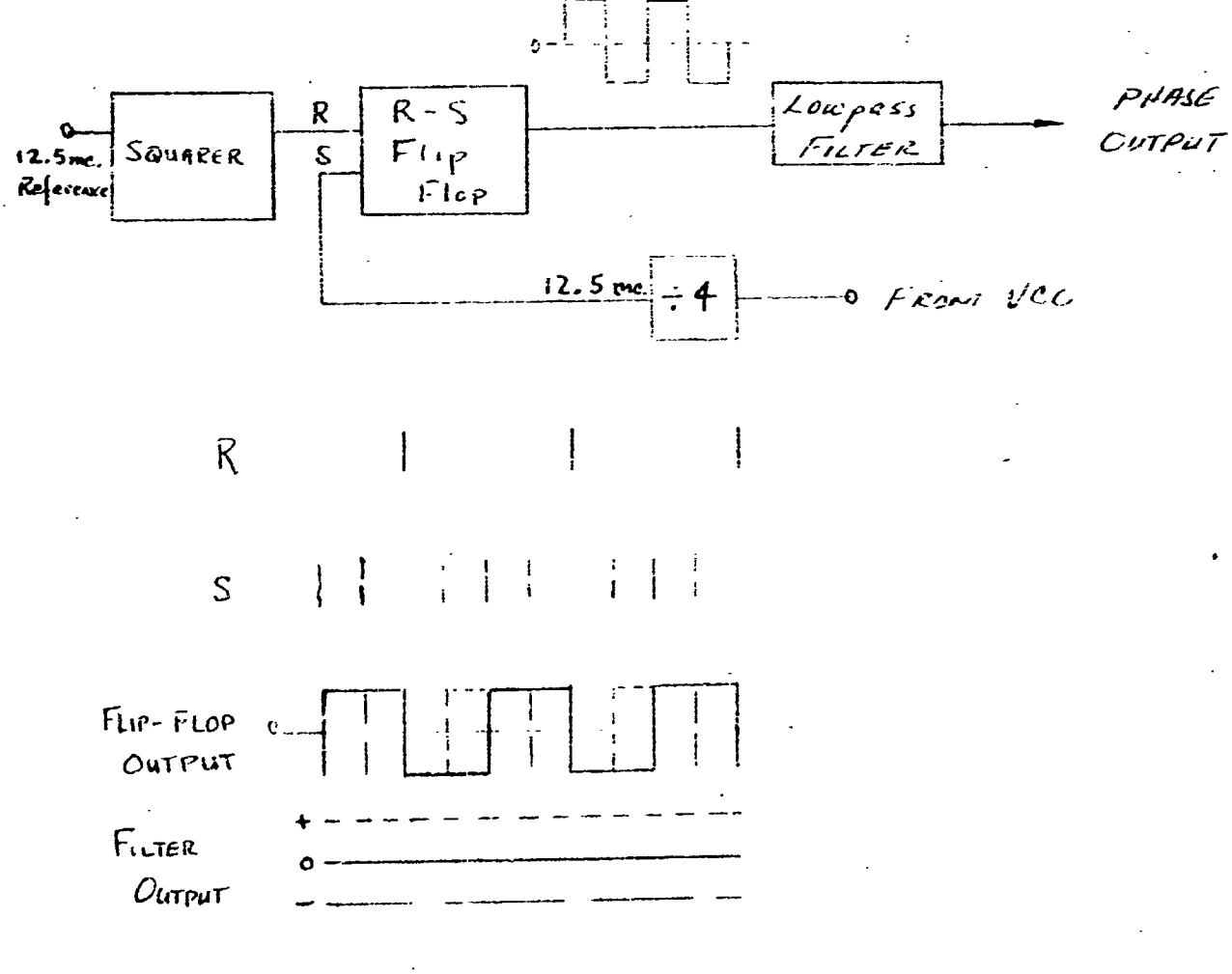

Figure 4.17 Block Diagram and Timing Diagram of Sawtooth Phase Comparator

The ideal phase comparator characteristic is shown in figure 4.18.

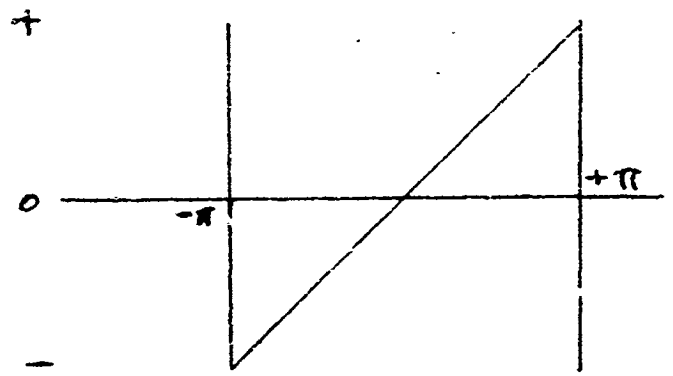

Figure 4.18 Ideal Sawtooth Comparator Characteristic

The ideal linear range extends from $-\pi$ to $+\pi$. The linearity of the saw is a function of the flip flop output waveform. The rise and fall times of the flip flop output cause the peaks of the sawtooth to be rounded and the pulse droop determines the ramp linearity. If a 2% linear ramp is required over the region $\pm$ 1 radian, the droop in the flip flop square wave must be 2% or less over the same portion of the wave form. The thin film flip flop referenced to earlier (maximum toggle speed 60 mc) can be forced to clamp in 5 nanoseconds after a set or reset pulse. The existing flip flop design is used in stroke logic and the waveform is not clamped at the positive level. The flip flop waveform droop is established by the clamp. The forecast thin film flip flop clamped waveform is shown in figure 4.19.

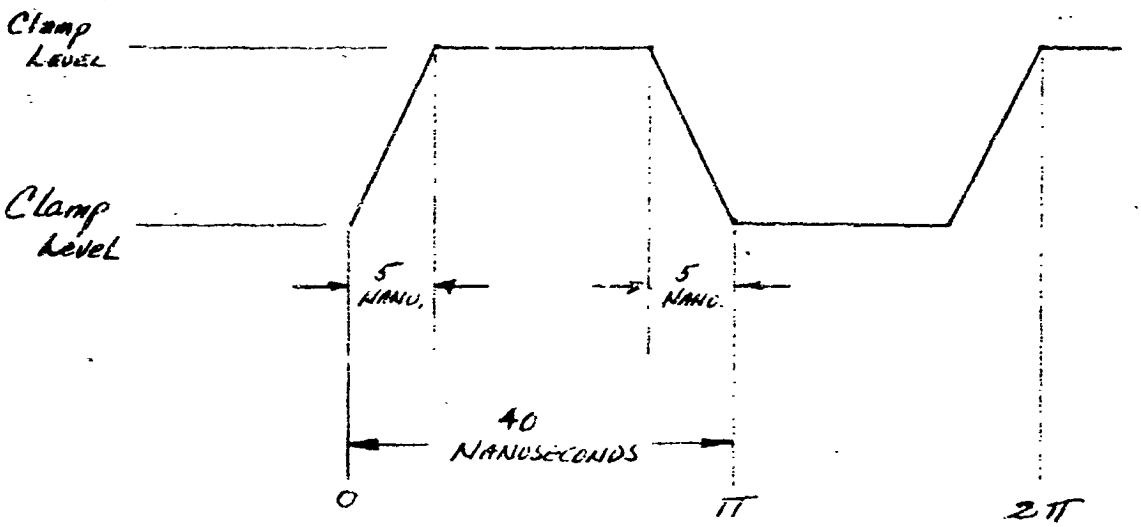

Figure 4.19 Thin Film Flip Flop Clamped Waveform

This form of the phase detector contributes a 5 nanoseconds delay. The ramp extends from $-\pi$ to $+\pi$. The phase comparator gain, Km, is fixed by the pulse amplitude and the ramp linearity is established by the clamp accuracy.

b. Early-Late-Gate Phase Detector

The block diagram of the Early-Late-Gate circuit is shown in figure 4.20.

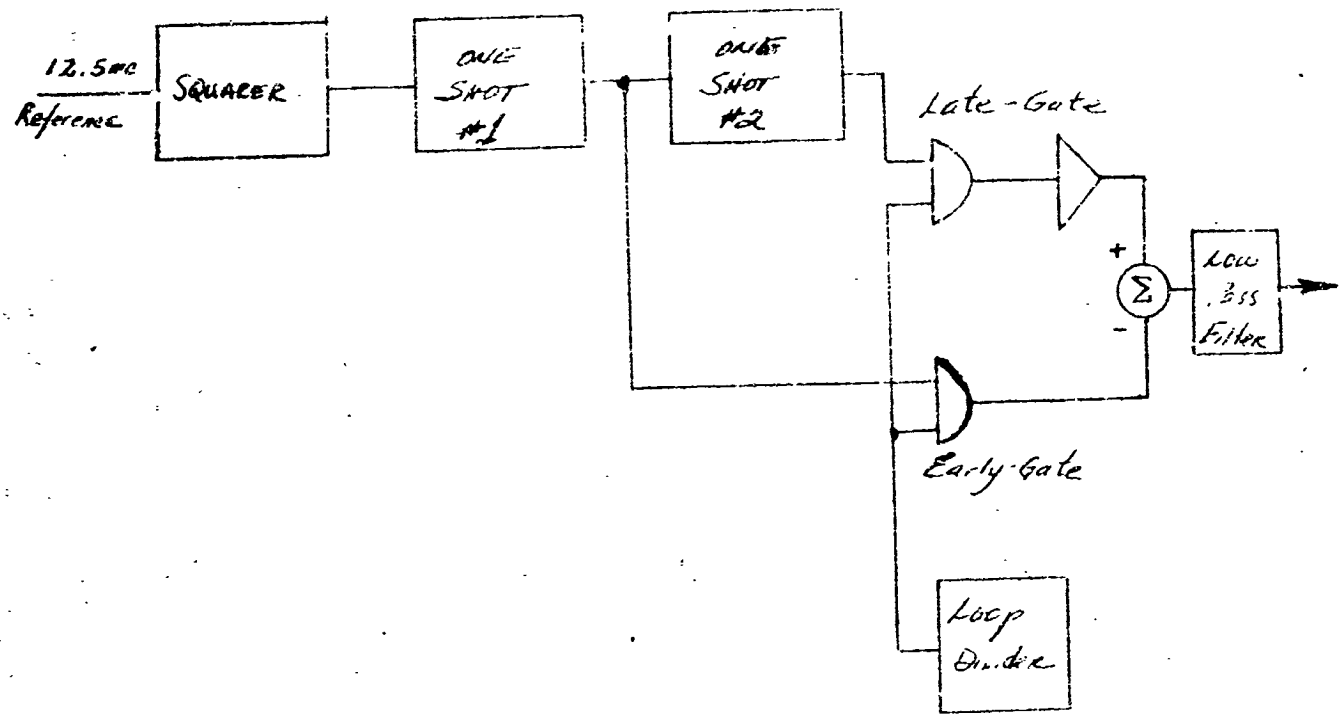

Figure 4.20 Simplified Block Diagram, Early-Late-Gate Phase Detector

The timing diagram is shown in figure 4.21.

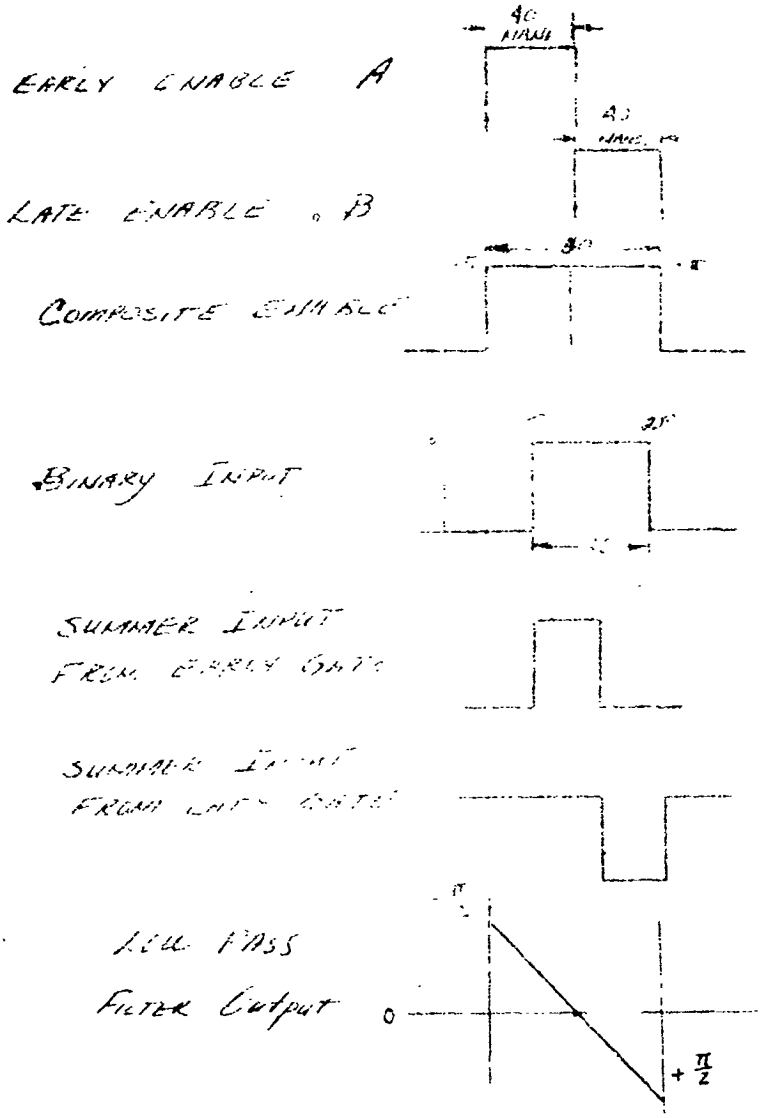

Figure 4.21 Timing Diagram of Early-Late-Gate Phase Detector

The system logic is as follows. The 12.5 mc reference enables an early-gate and late-gate as shown. If the loop static phase error is zero, the binary input pulse from the divider is centered and half the pulse energy falls within the early-gate and half in the late-gate. The late gate output is inverted and summed with the early-gate output.

For zero static phase error the summer output is zero. If the VCO phase advances with respect to the reference phase, the system waveforms change as indicated in figure 4.21. If the VCO phase is retarded with respect to the reference phase the inverse process occurs. The summer output is the correlation function of the reference and binary pulse. Ideally, this phase detector is linear over the region $-\frac{\pi}{2}$ to $+\frac{\pi}{2}$. The additional (approximately 10 nanoseconds) loop time delay is attributed to the early-gate late-gate and inverter. The linearity of the phase detector characteristic is determined by the droop in the gate output wave forms.

c. Modulo-Two Adder Phase Detector

The third form of the phase detector considered consists of a positive and negative Modulo Two Adder (Exclusive OR Gate) whose outputs are summed. The simplified diagram of this system is shown in figure 4.22.

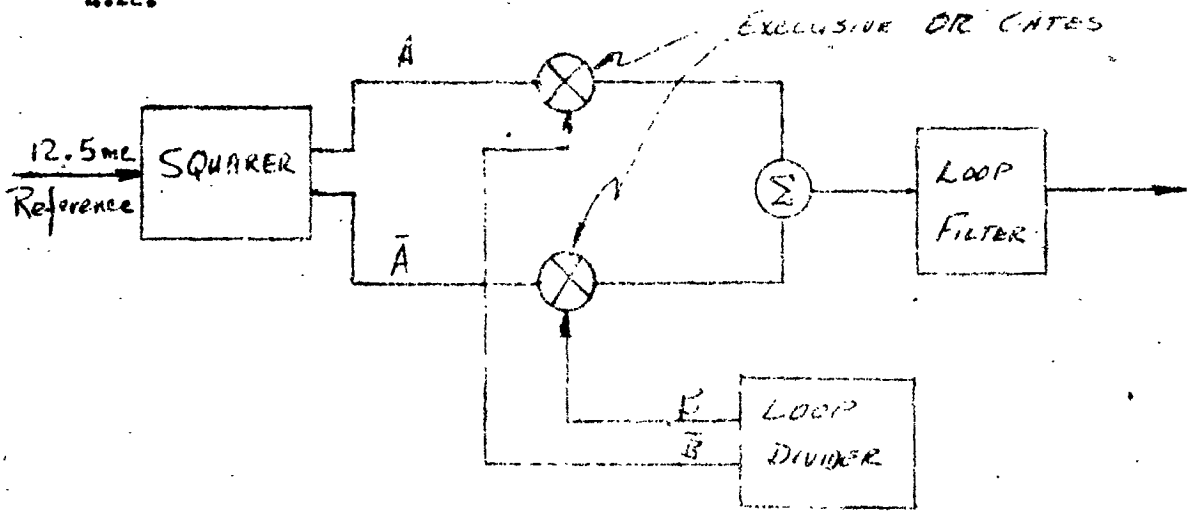

Figure 4.22 Simplified Diagram of Mod. 2 Adder Phase Detector

The autocorrelation function of this system is shown in figure 4.23.

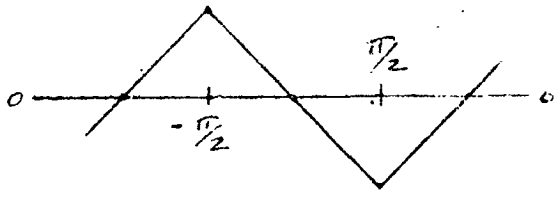

Figure 4.23 Autocorrelation of Modulo Two Adder

The linearity of the ramp shown is determined by the gate output waveforms. The ideal linear region extends from + $\pi/2$ to - $\pi/2$. The delay of the gates and inverter is approximately 10 nanoseconds.

d. Conclusion

The principal phase detector parameters include 1) Linearity over the region ± 1 radian. 2) Delay 3) Simplicity 4) 12.5 Mc/s rejection. The type of phase comparator that appears to be most promising is the Flip Flop Sawtooth Phase Comparator because its ideal linear region is twice that of the Early-Late-Gate and Modulo-Two Adder. Further, this unit exhibits minimum delay, its linearity is determined by clamp accuracy and it is much simpler than the others considered. However, at zero phase error, the Early-Late-Gate and the Mod-Two Adder circuits give output waveforms with small 12.5 Mc/s content, whereas the Flip-Flop Comparator yield a 12.5 Mc/s squarewave. At a ± $\pi/2$ phase shift, the former circuits produce a 12.5 Mc/sec square wave while the Flip-Flop circuit gives a 3:1 ratio 12.5 Mc/s wave. The 12.5 Mc/s content of the Flip-Flop comparator approaches zero as the phase approaches ± π.

This weakness of the Flip-Flop comparator may be circumvented by using two Flip-Flops, driven by the inverse outputs from the Divider chain and the reference squarer. This gives two identical output waveforms displaced 40 nanoseconds in time which may be summed and filtered by the loop. At all phase errors the 12.5 Mc/s content is now zero, except for a small amount due to an unbalance in circuit delays, amplitudes and waveforms. The fundamental frequency in the sum is 25 Mc/s. This has minimum amplitudes at phase errors of 0 and $\pm \pi$, with maximum at $\pm \pi/2$.

An alternative approach would be to cut the frequency divider to $\div$ 2 and to run the phase detector at 25 Mc/s frequency. This would give a zero 12.5 Mc/s output, but would require the linearity of the phase detector to be adequate over $\pm$ 2 radians.

Either method enables the 12.5 Mc/s leak to be reduced and also reduces the transport and ramping delays associated with the digital phase divider and detector.